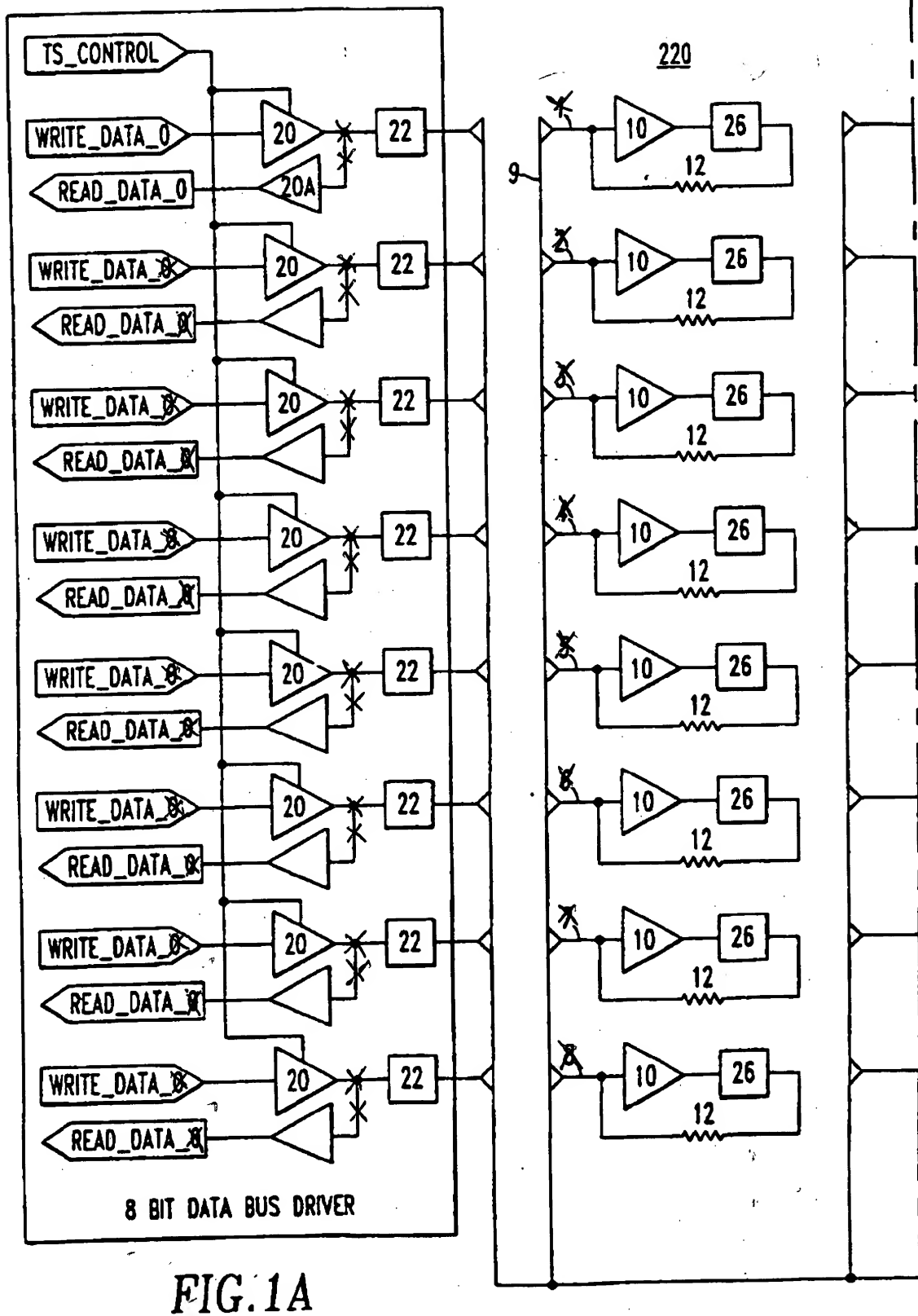




OK to enter



BEST AVAILABLE COPY

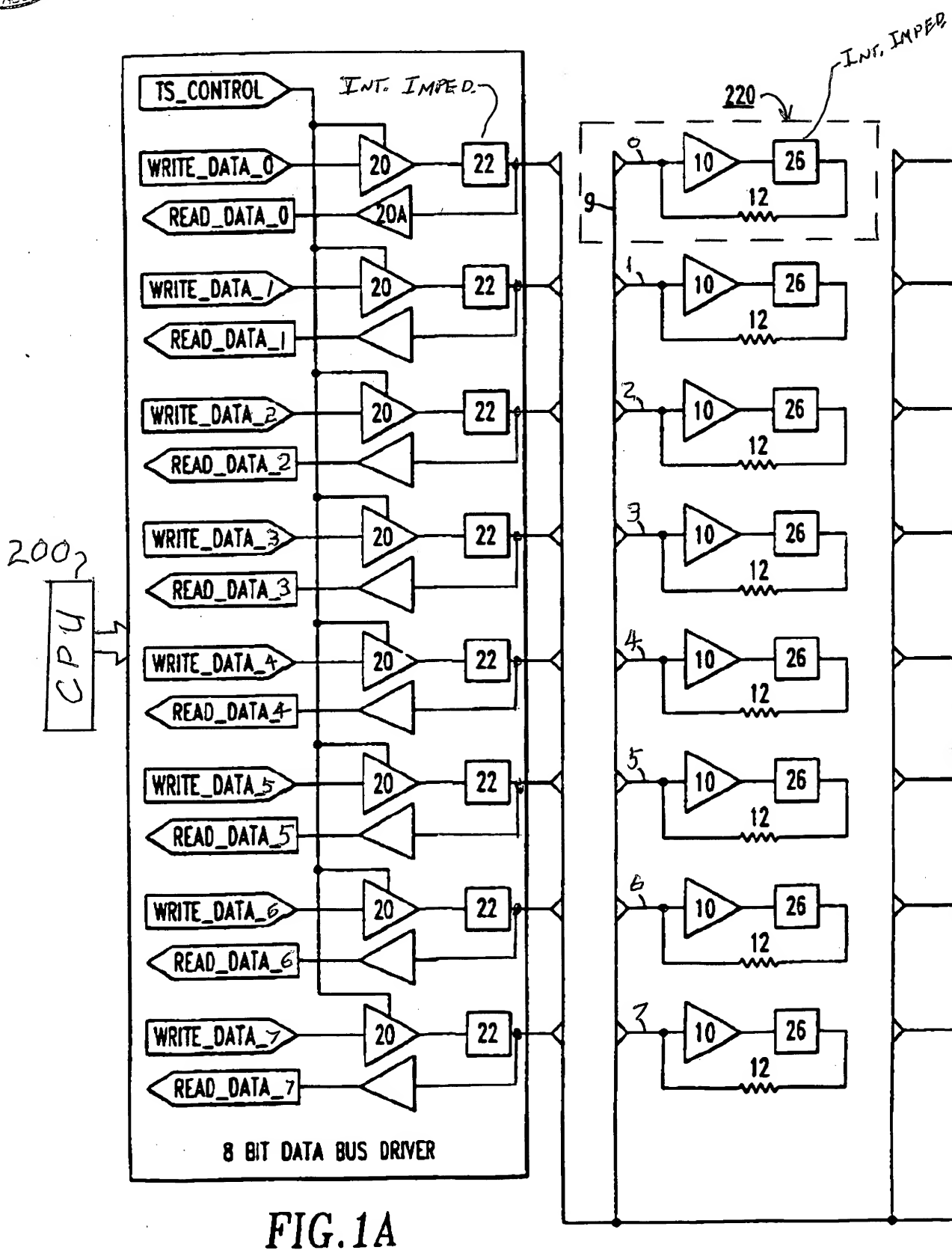
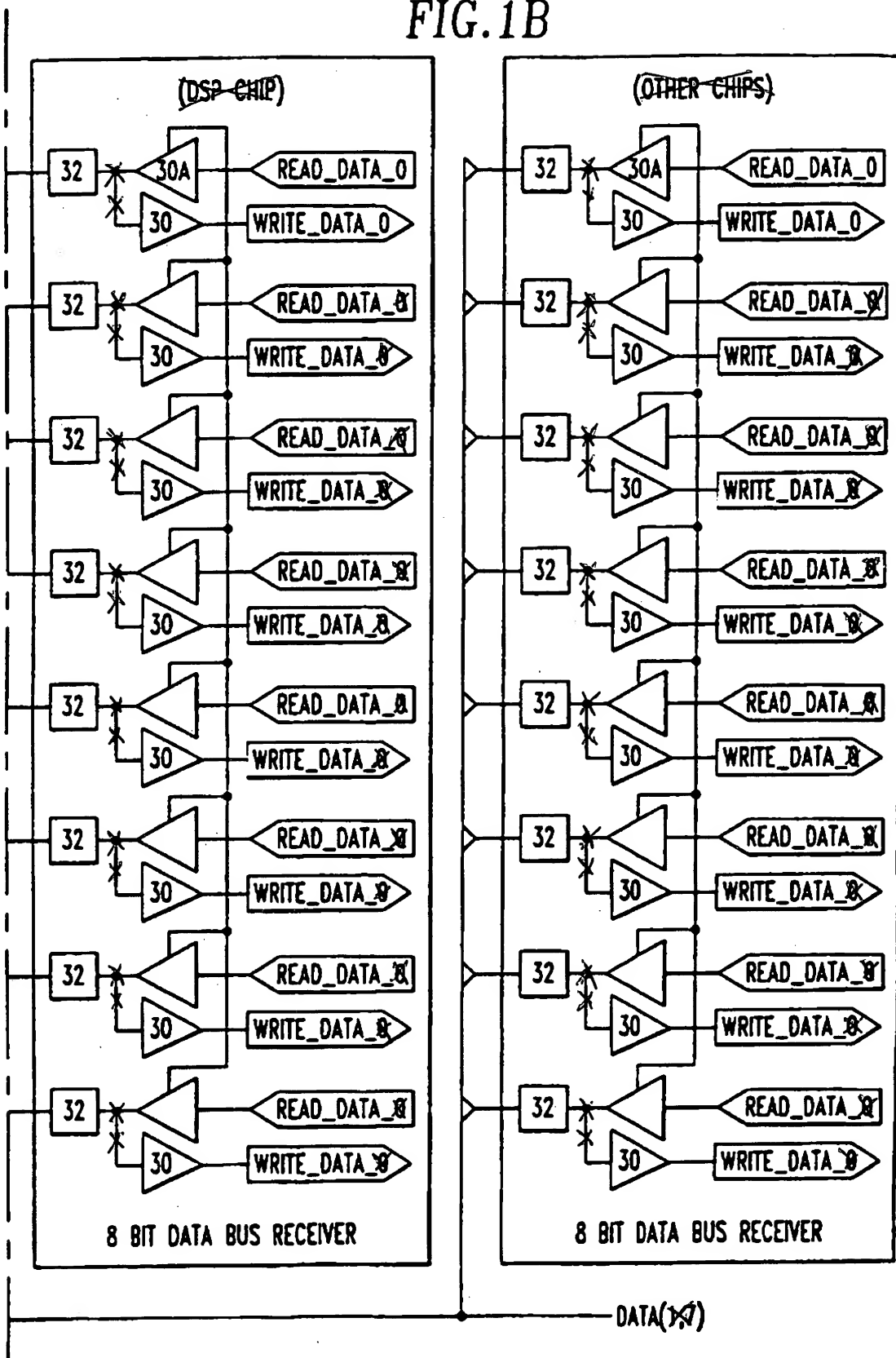
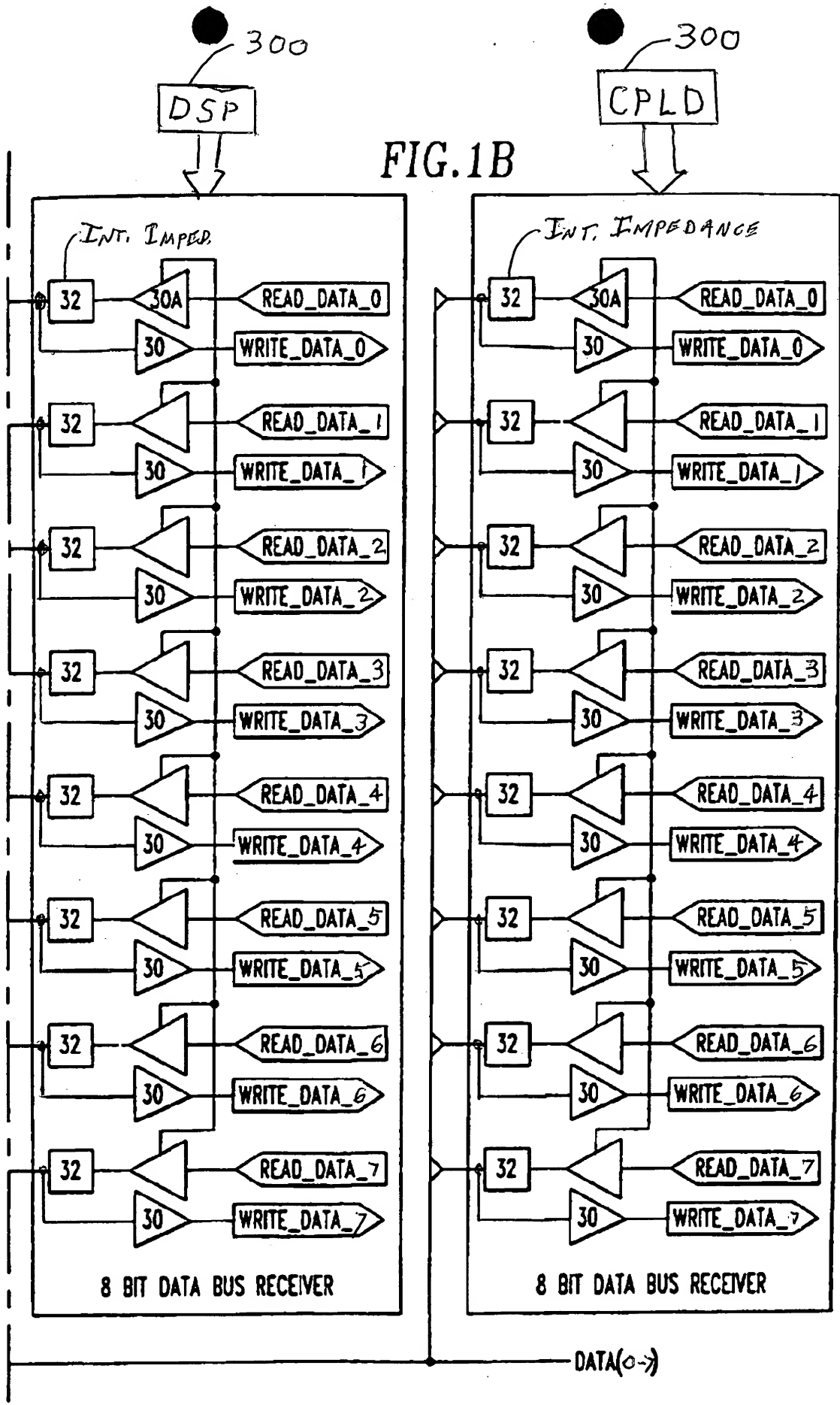




FIG. 1B







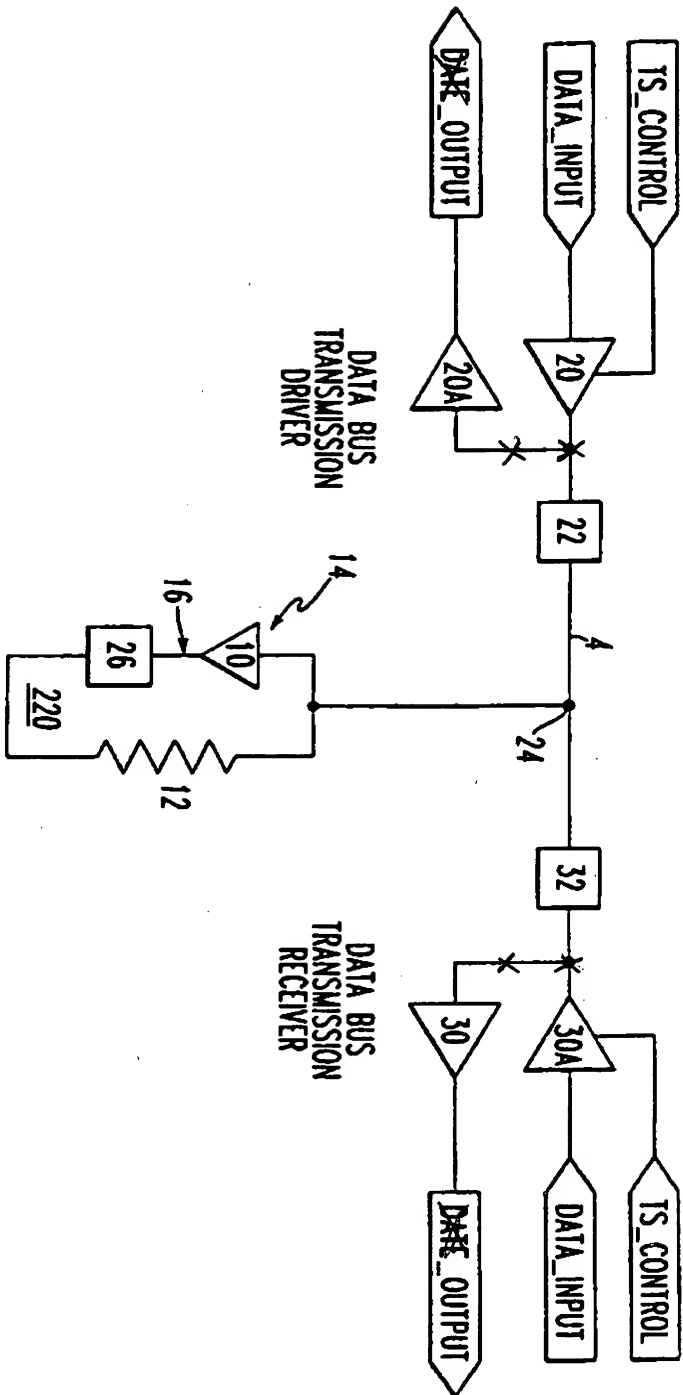
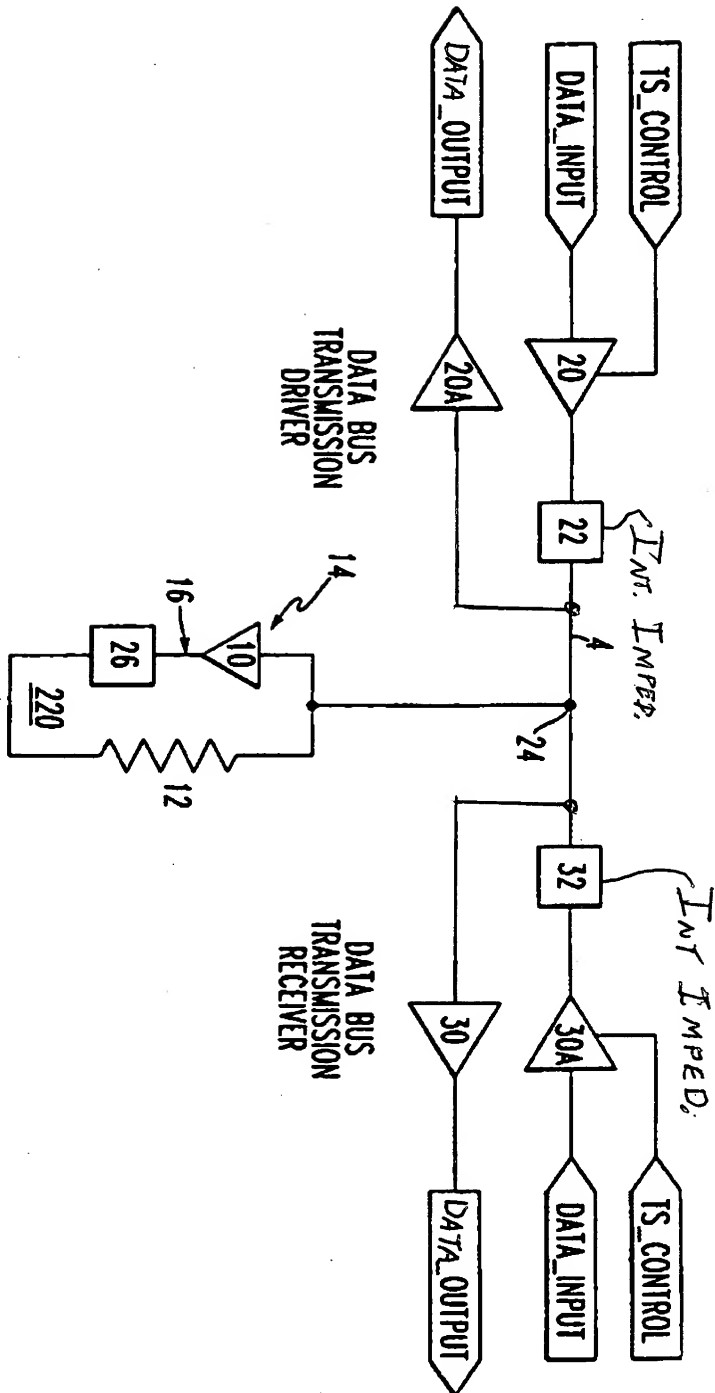
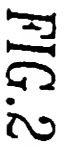


FIG.2



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FIGURE 3A  
(Prior Art)

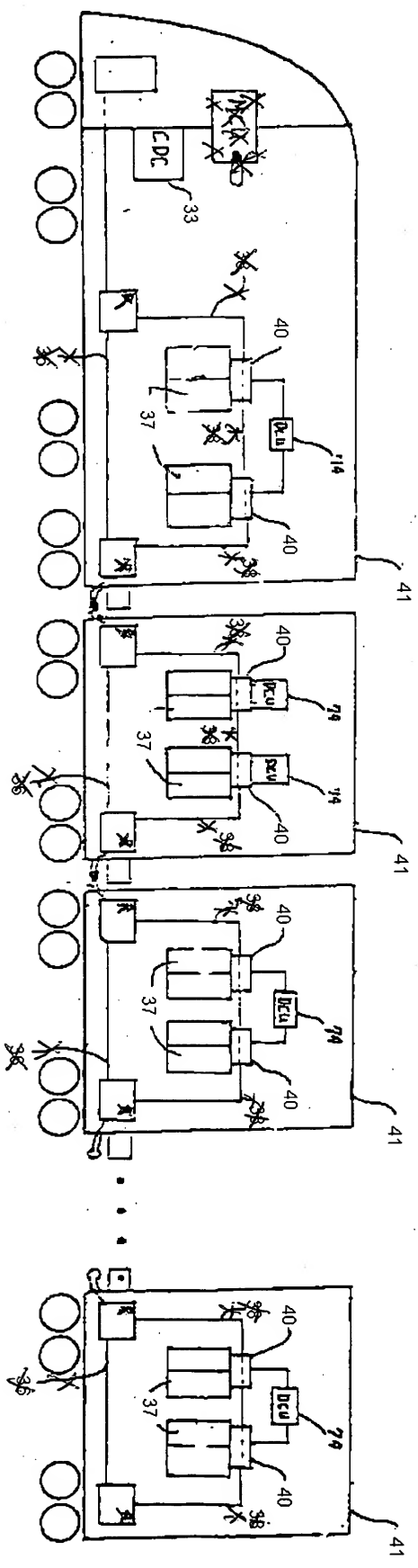
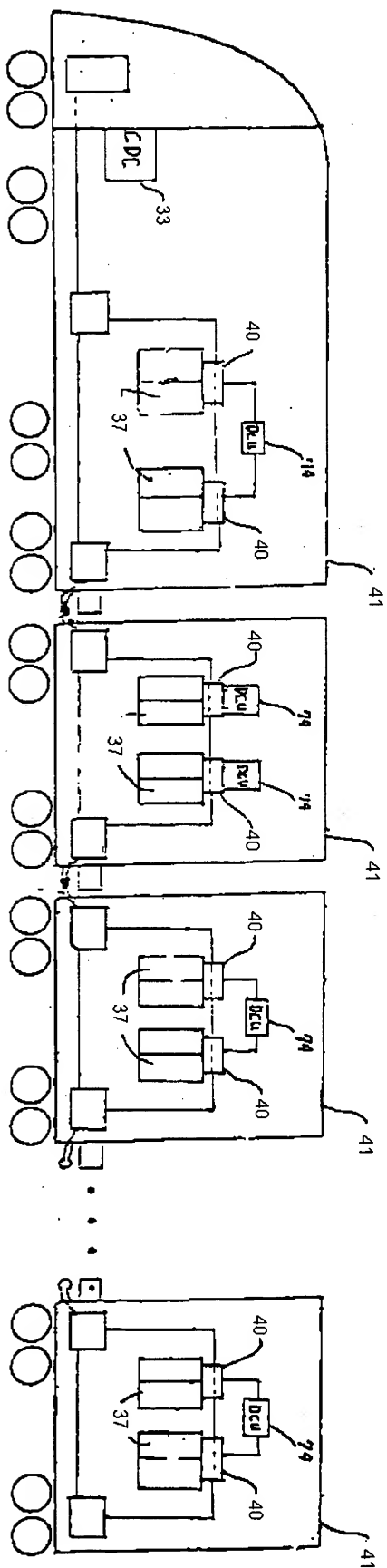




FIGURE 3A  
(Prior Art)



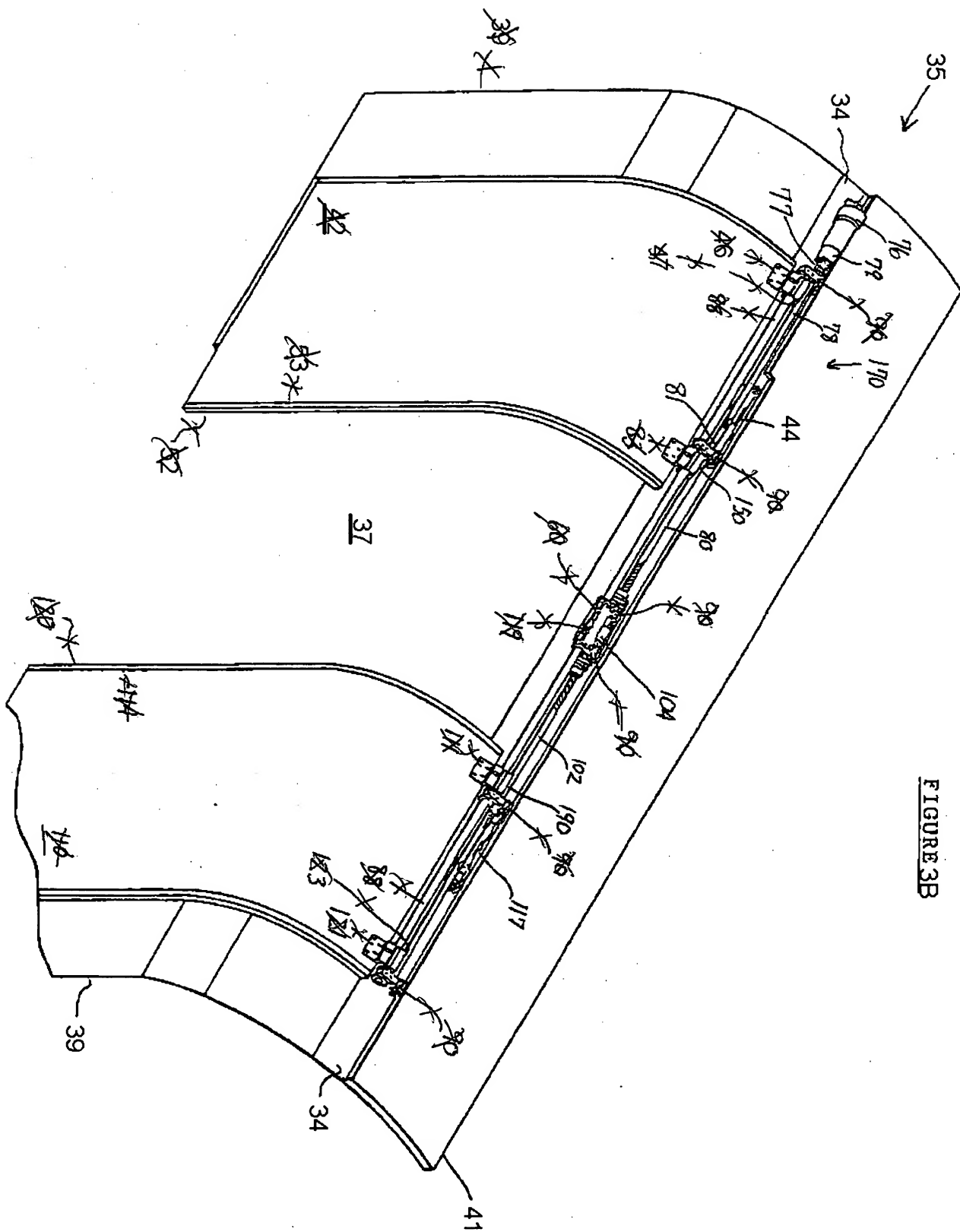


FIGURE 3B

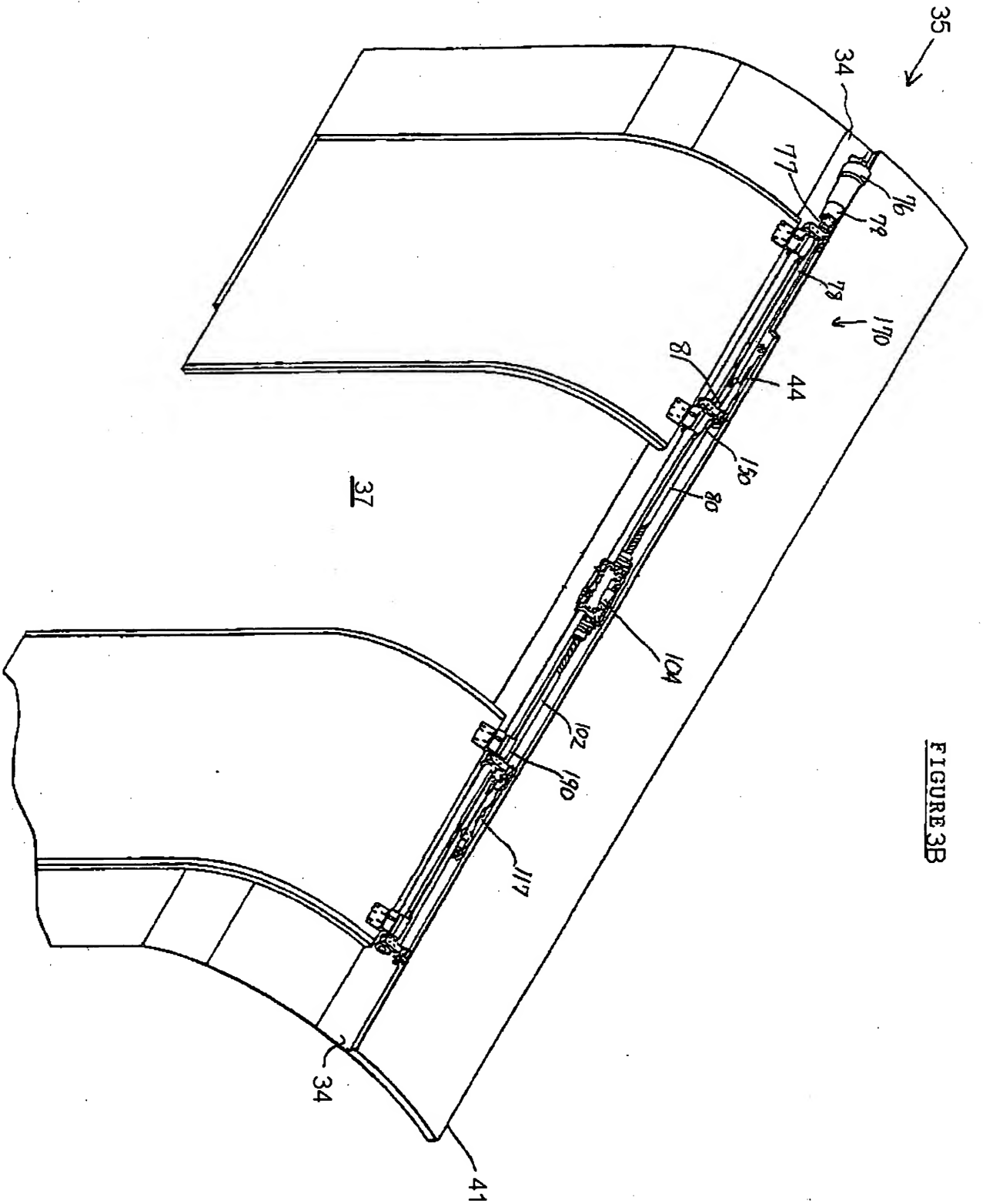
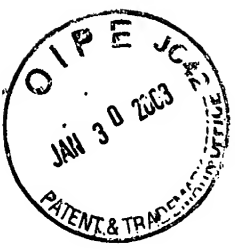


FIGURE 3B

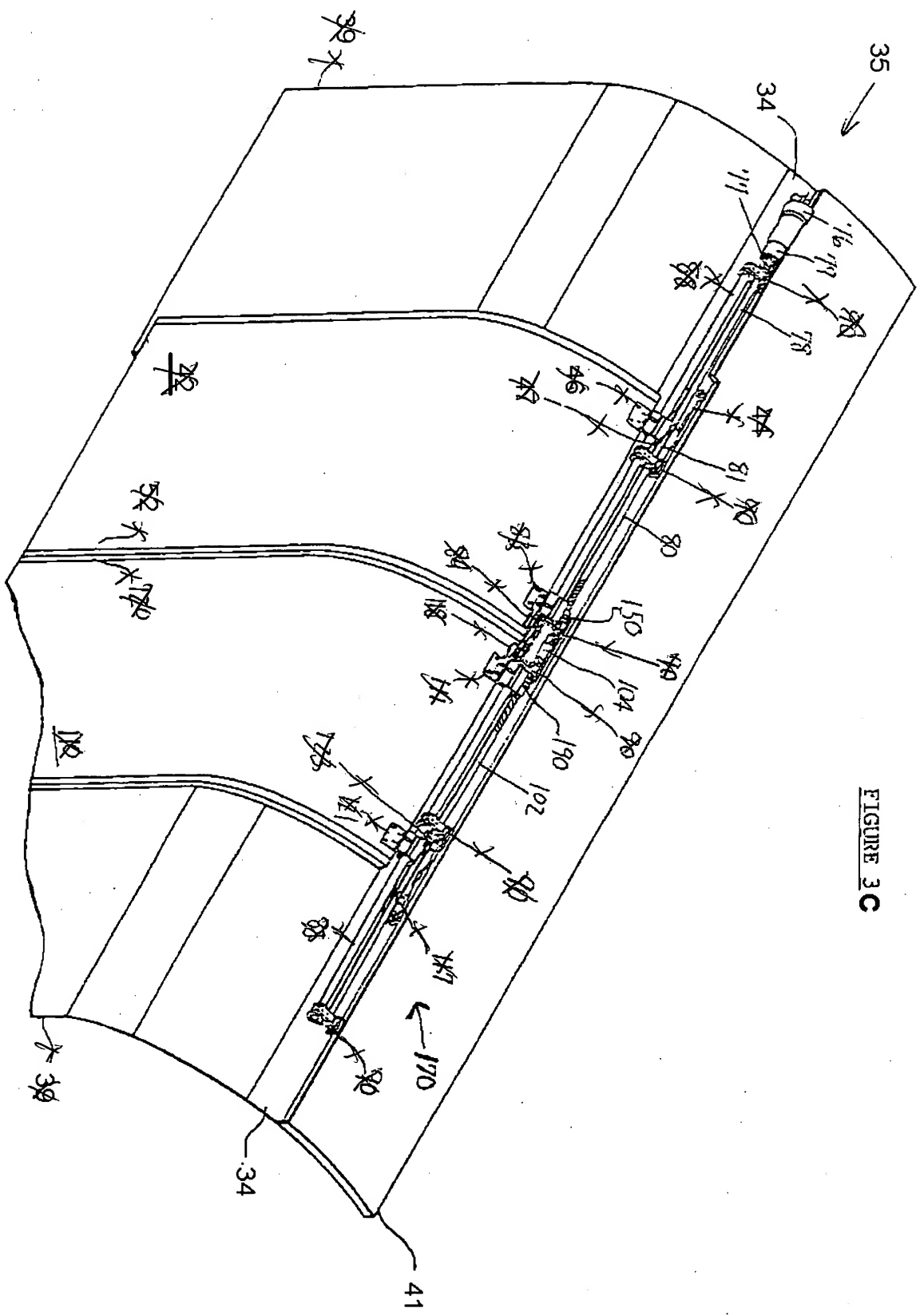
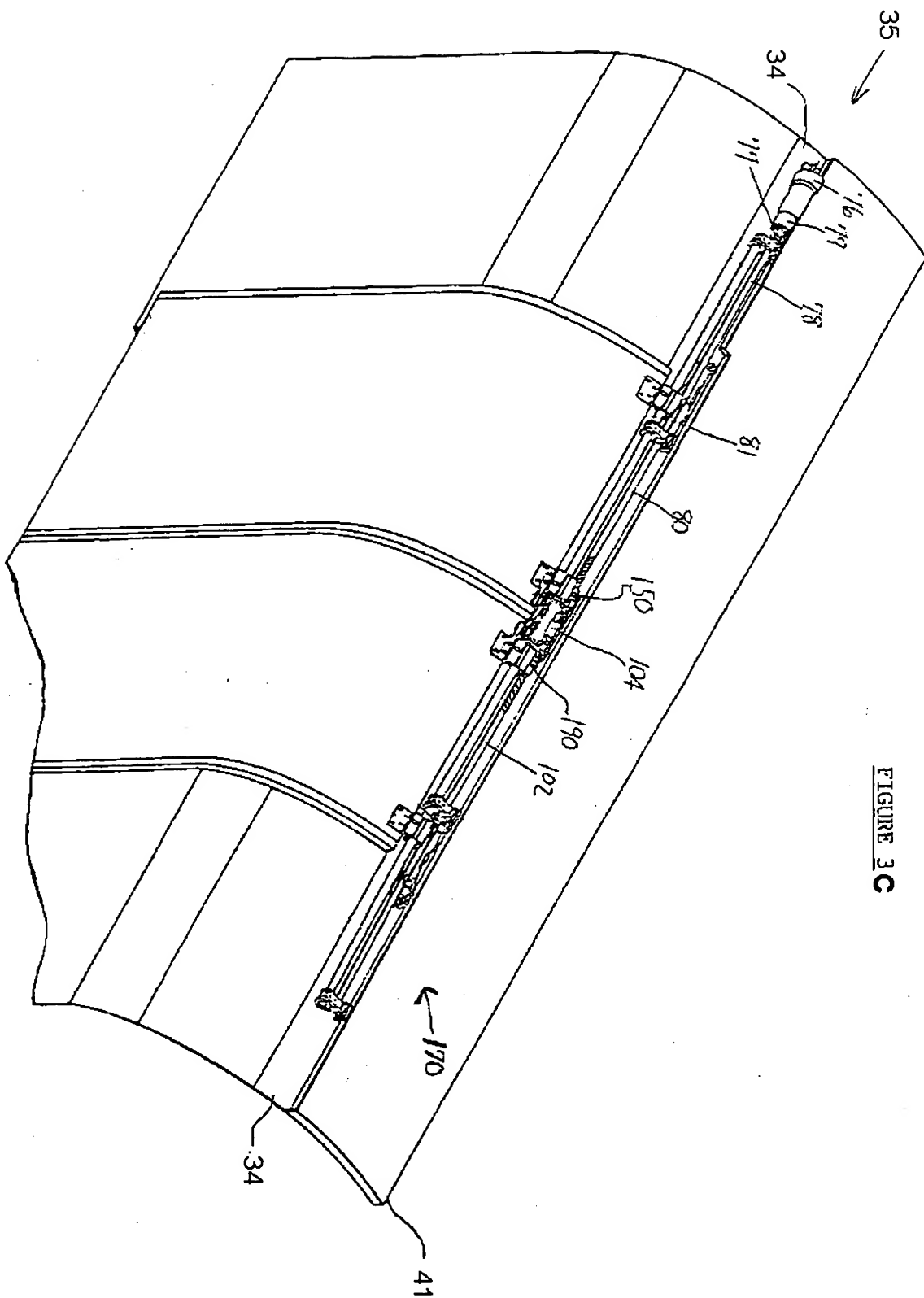
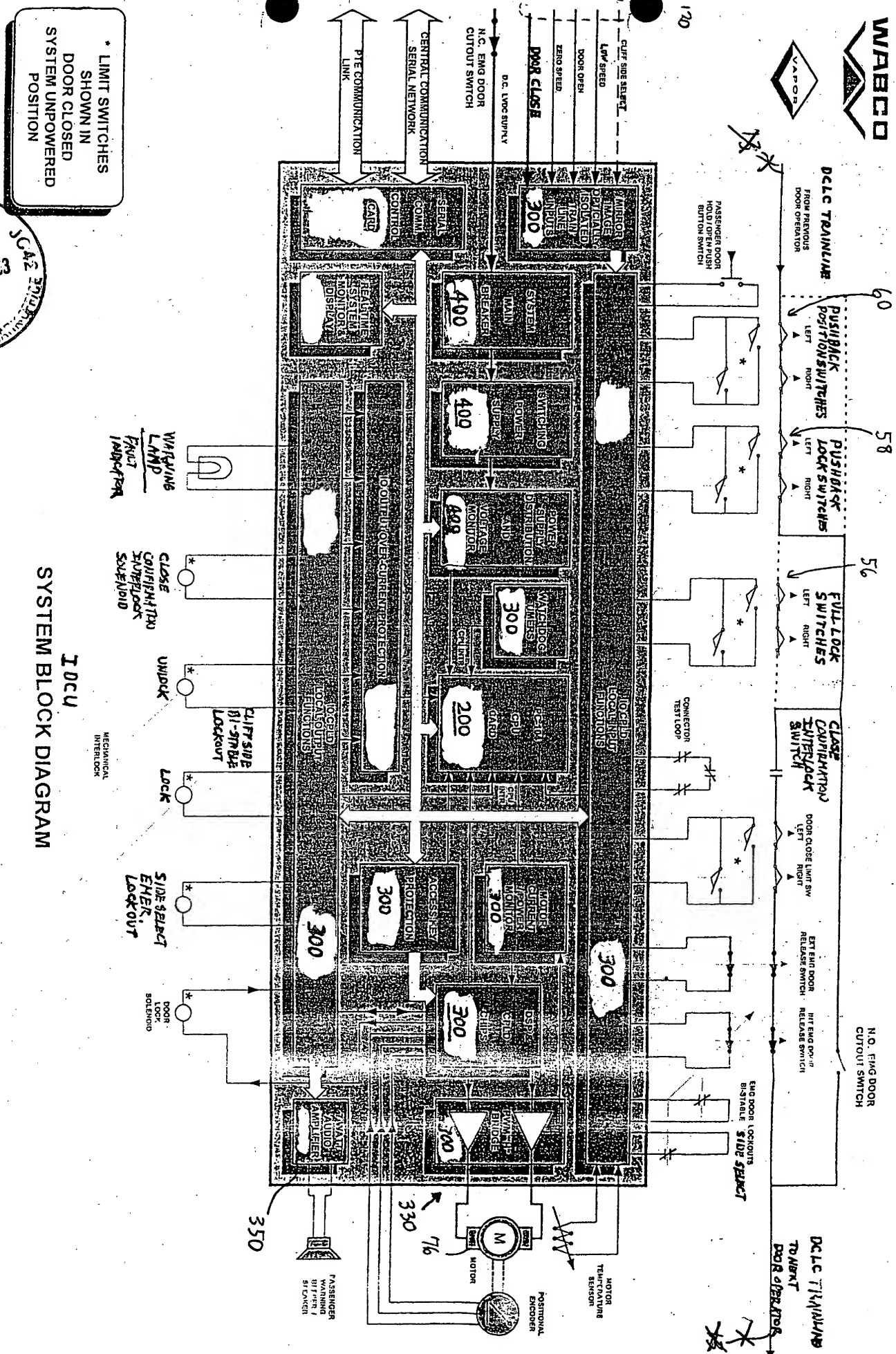


FIGURE 3C



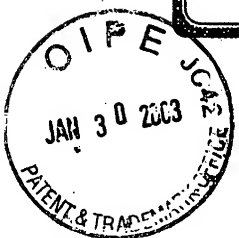
**FIGURE 3C**





# 10cy SYSTEM BLOCK DIAGRAM

\* LIMIT SWITCHES  
SHOWN IN  
DOOR CLOSED  
SYSTEM UNPOWERED  
POSITION

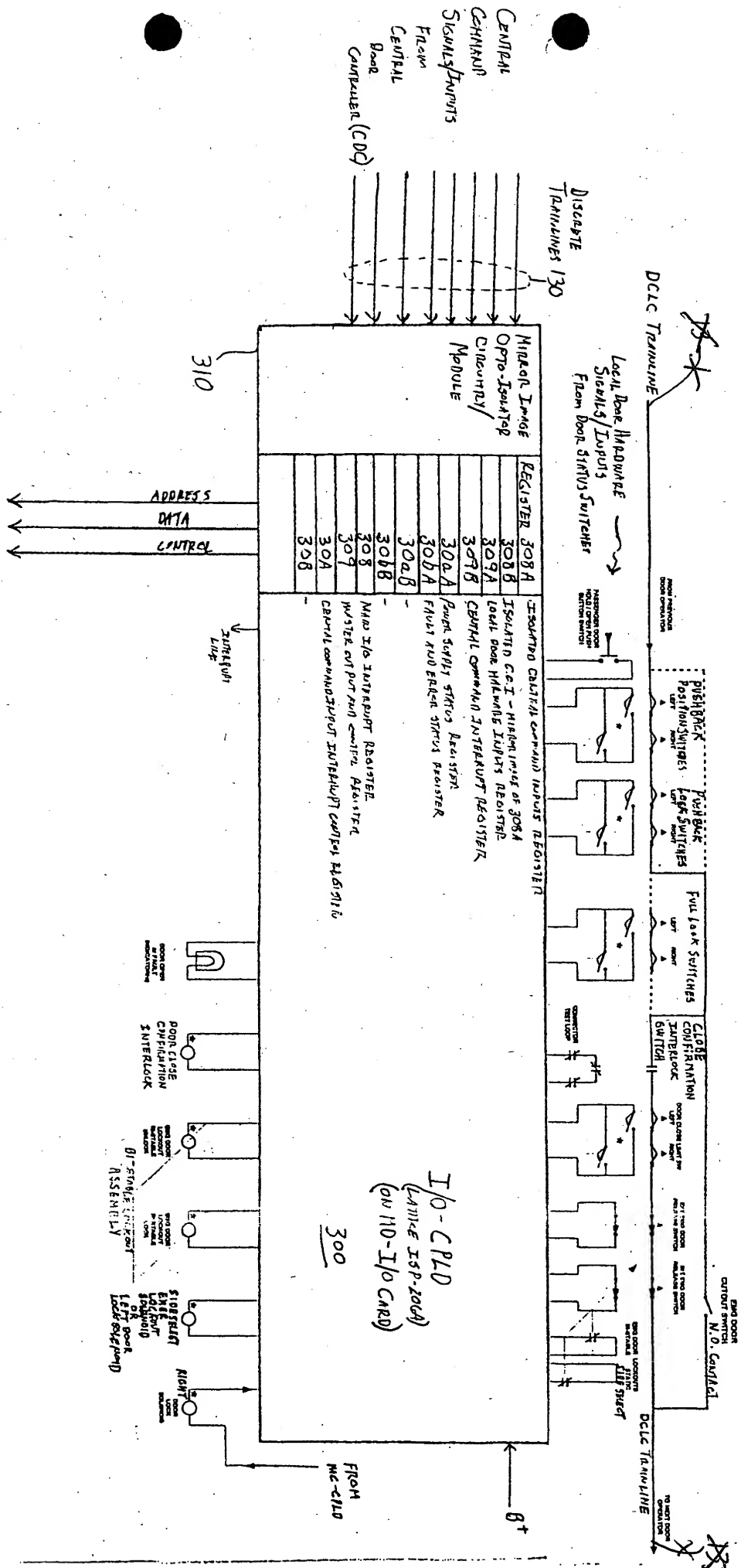




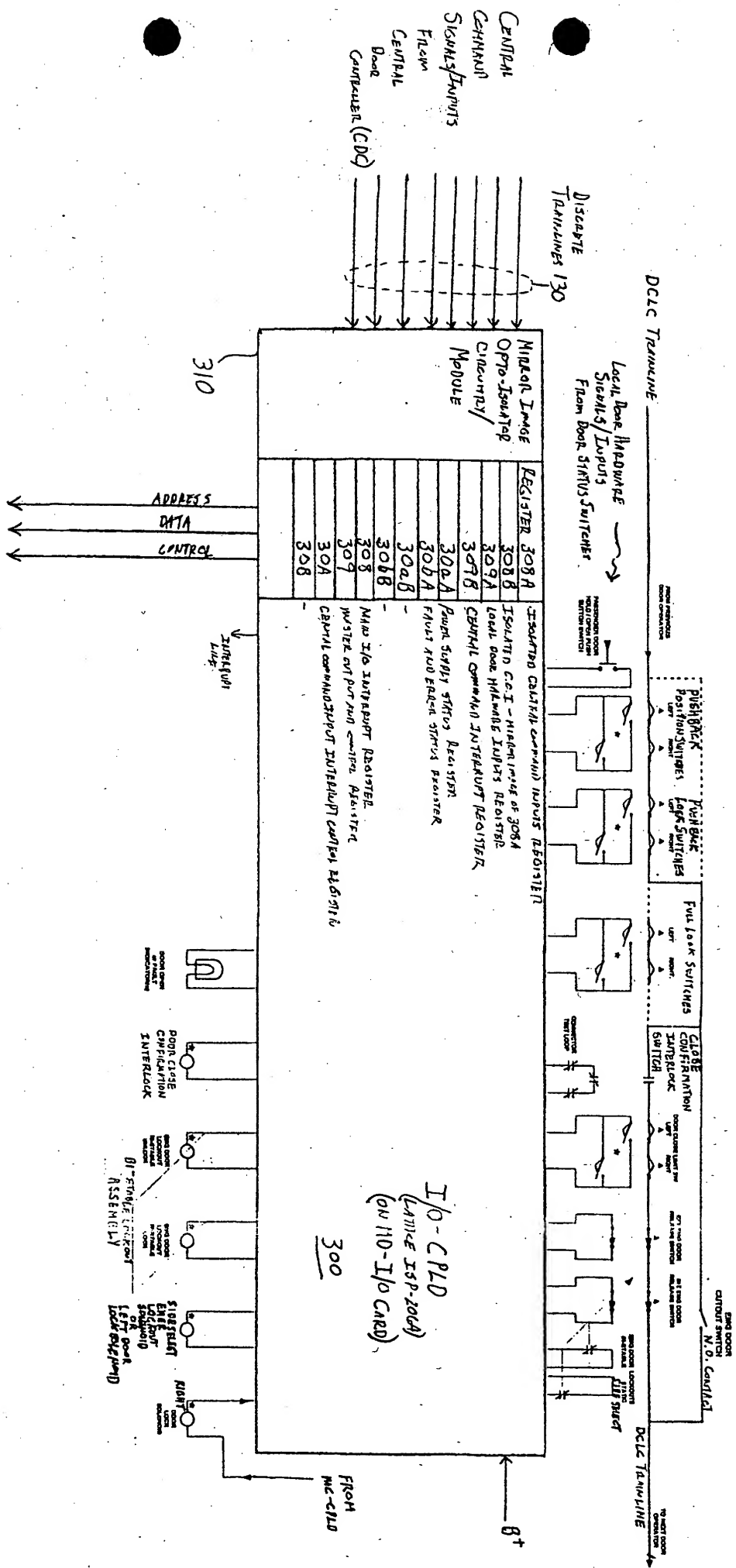
• LIMIT SWITCHES  
SHOWN IN  
DOOR CLOSED  
SYSTEM UNPOWERED  
POSITION



FIGURE 7A



**FIGURE 5 A**





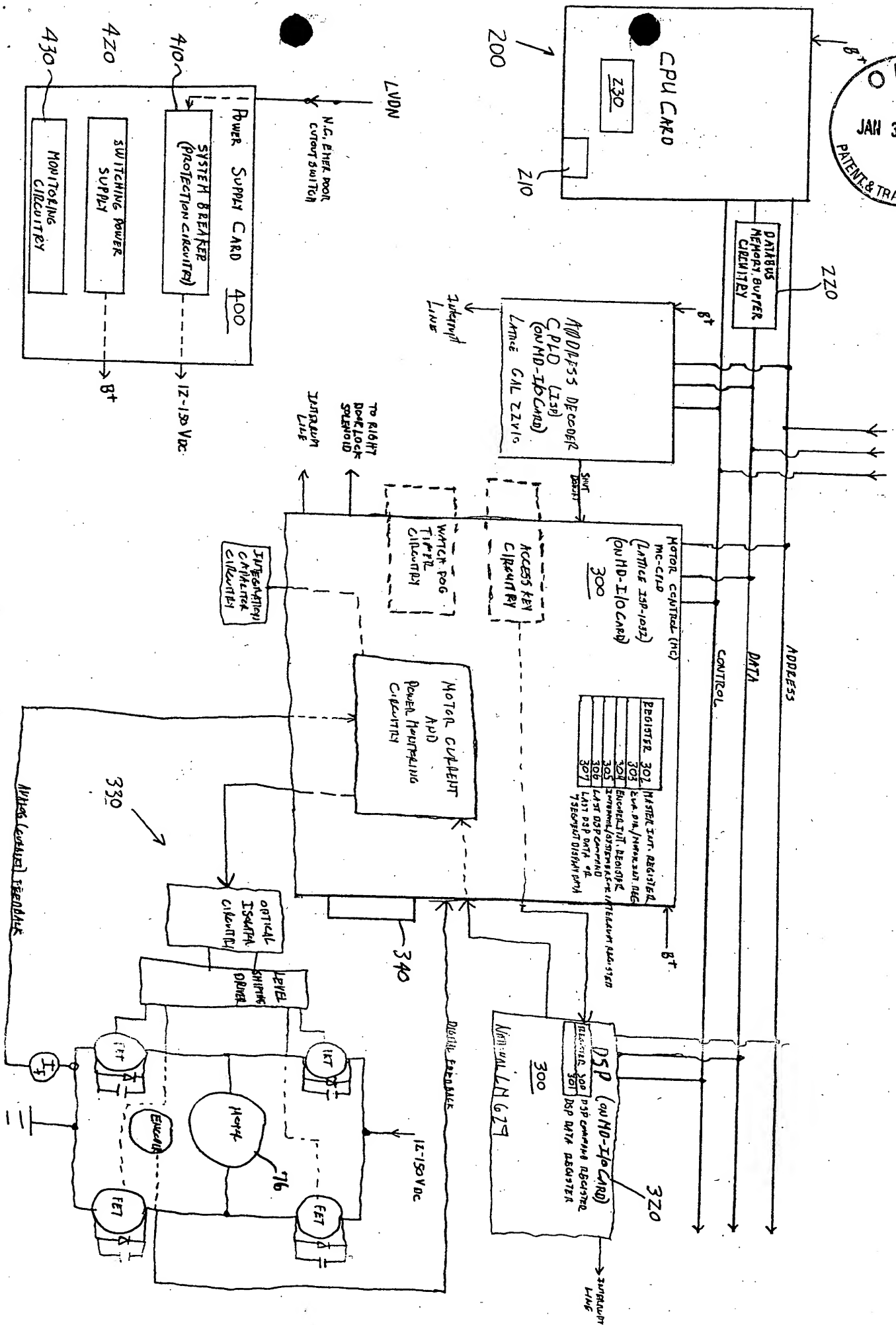




FIGURE 8

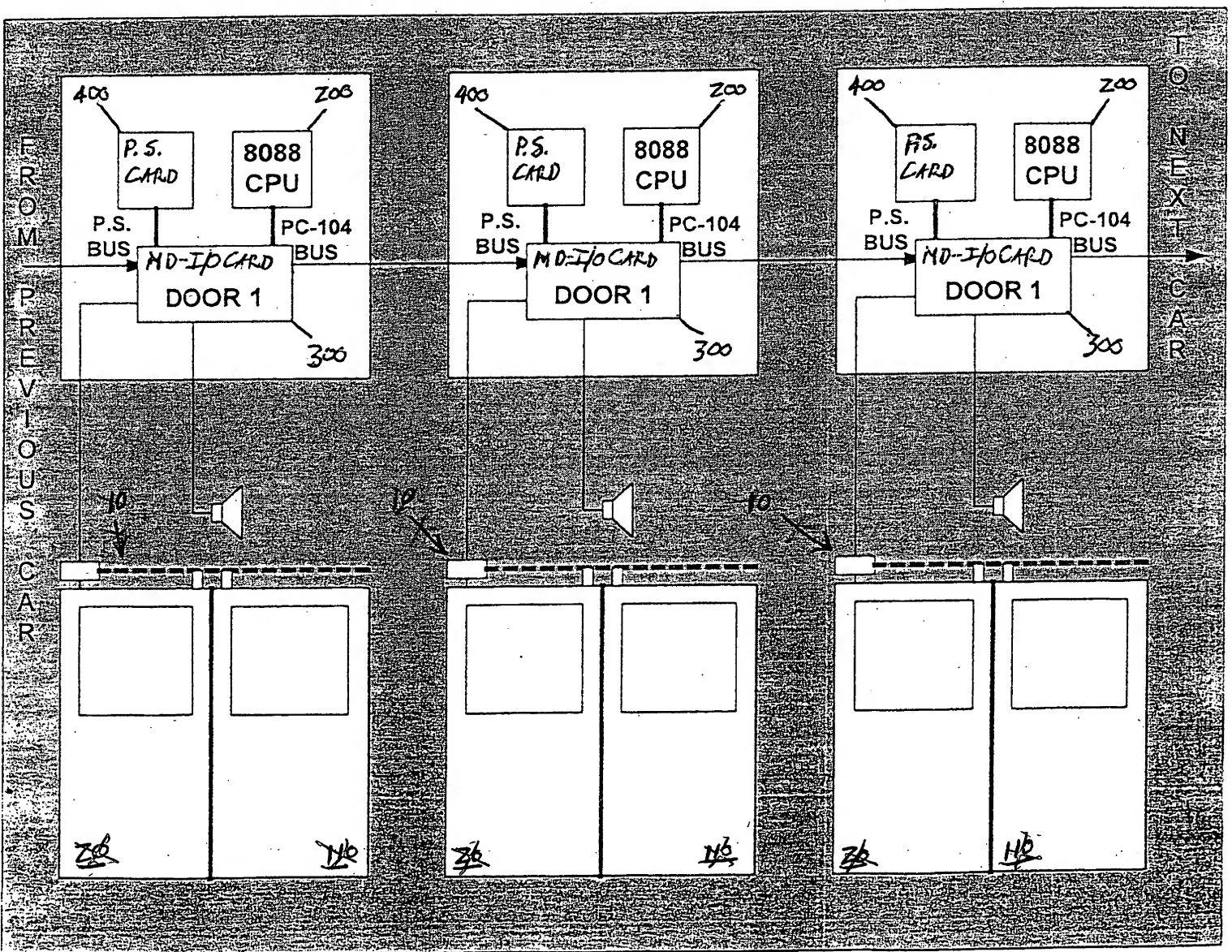






FIGURE 6

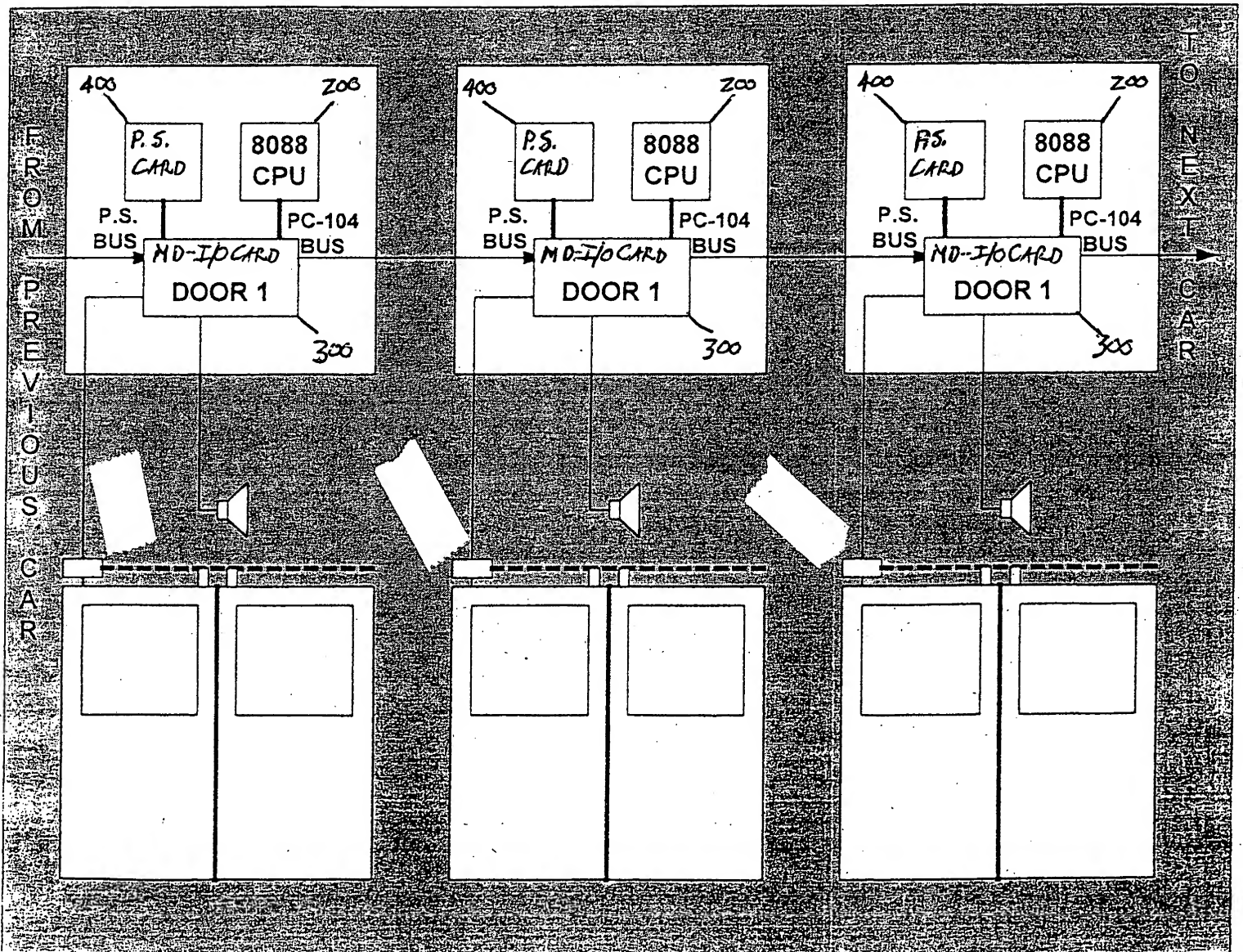




FIGURE 3

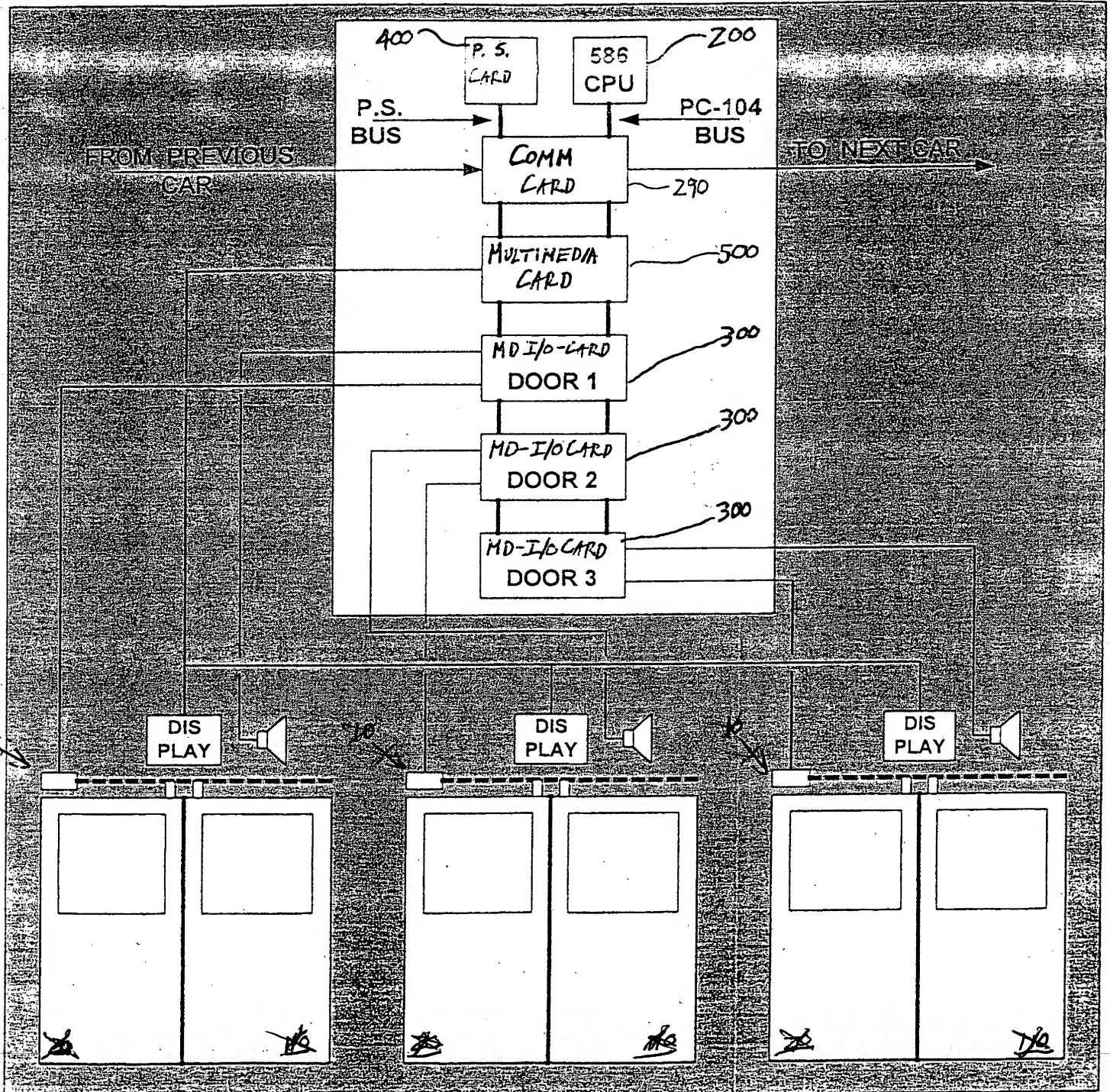
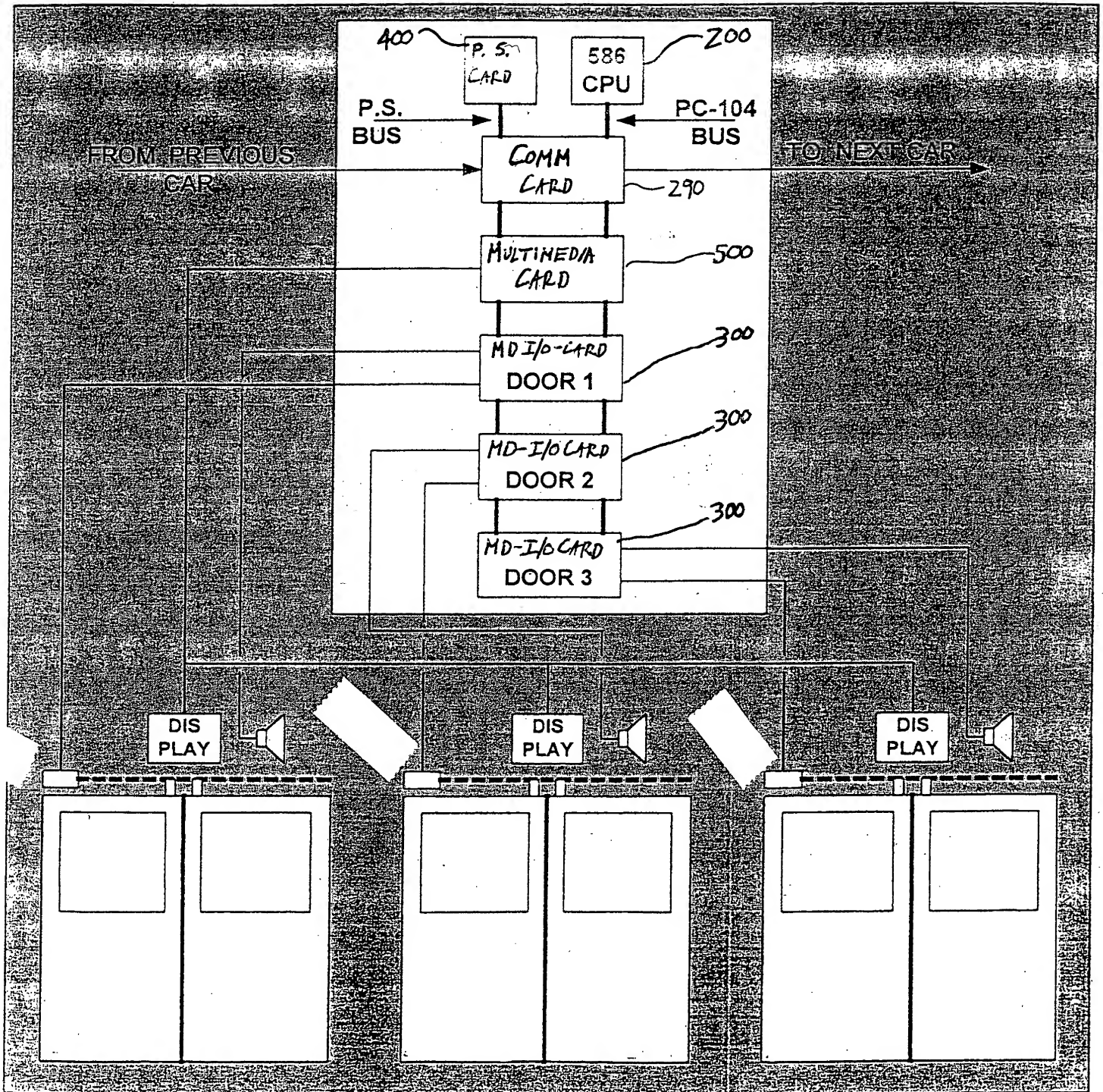


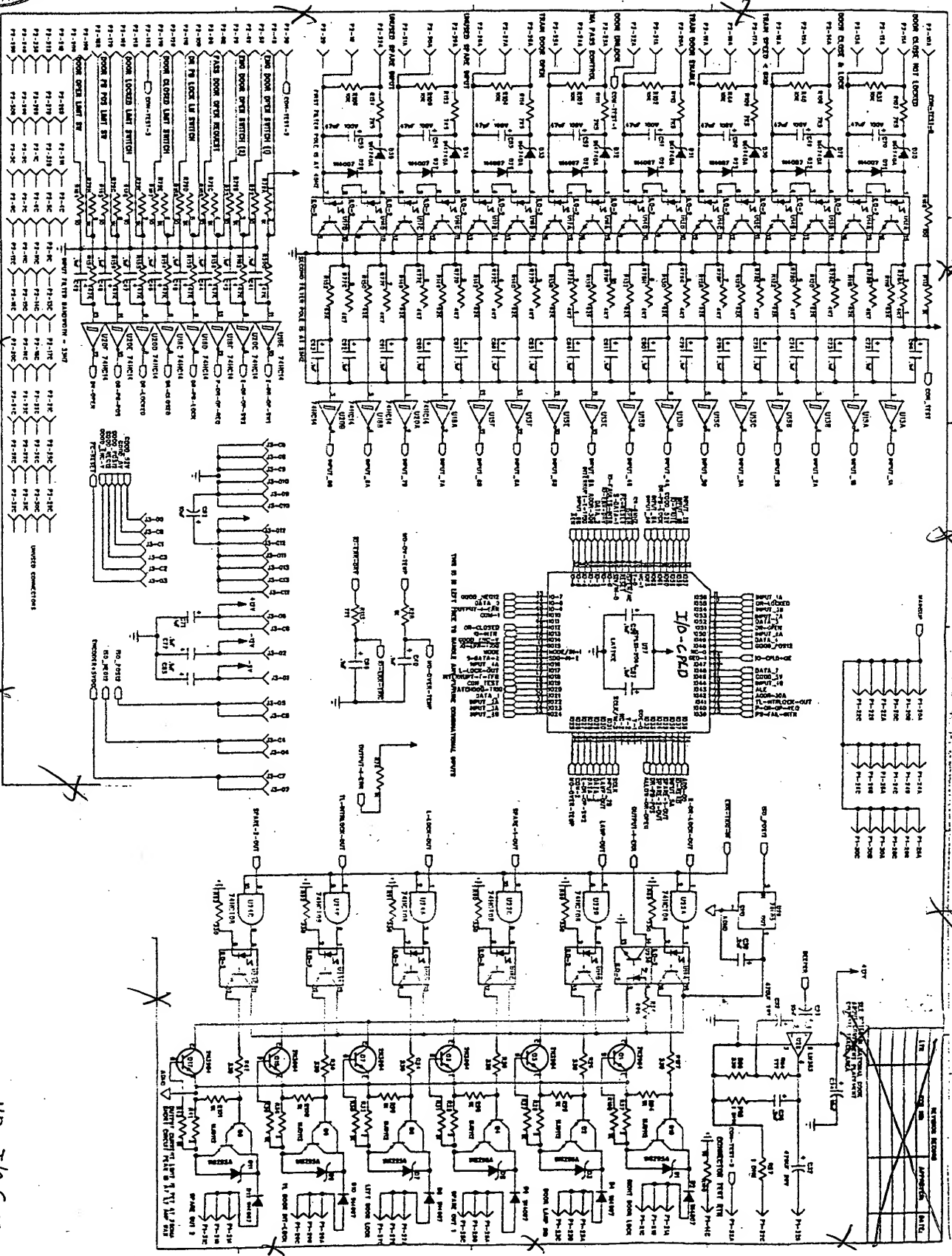
FIGURE 7



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FIGURE 310A

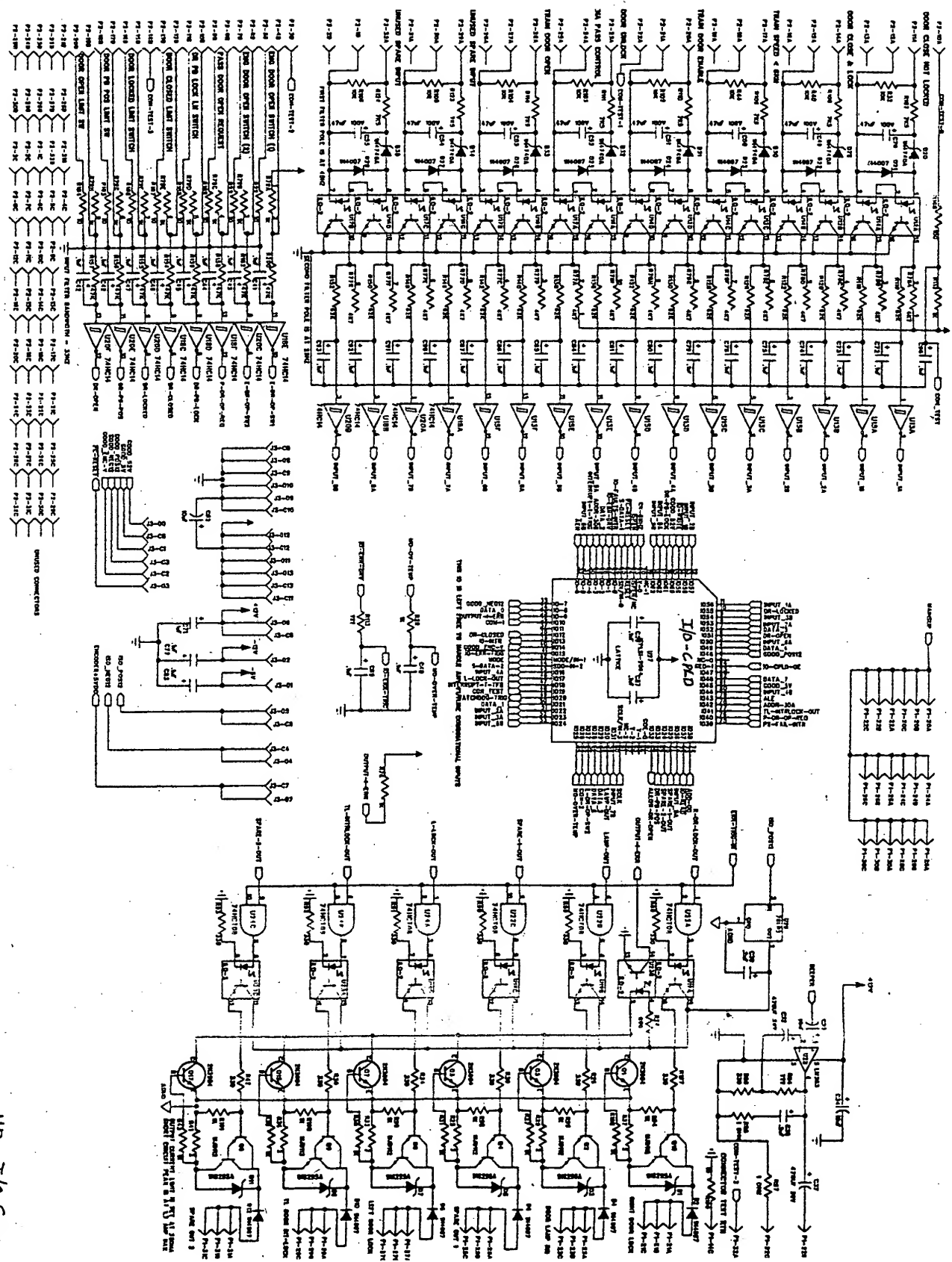


MD-I/O CARD  
 Layout 1

O I P E JC42-270  
 JAN 30 2003  
 PATENT & TRADEMARK OFFICE

310

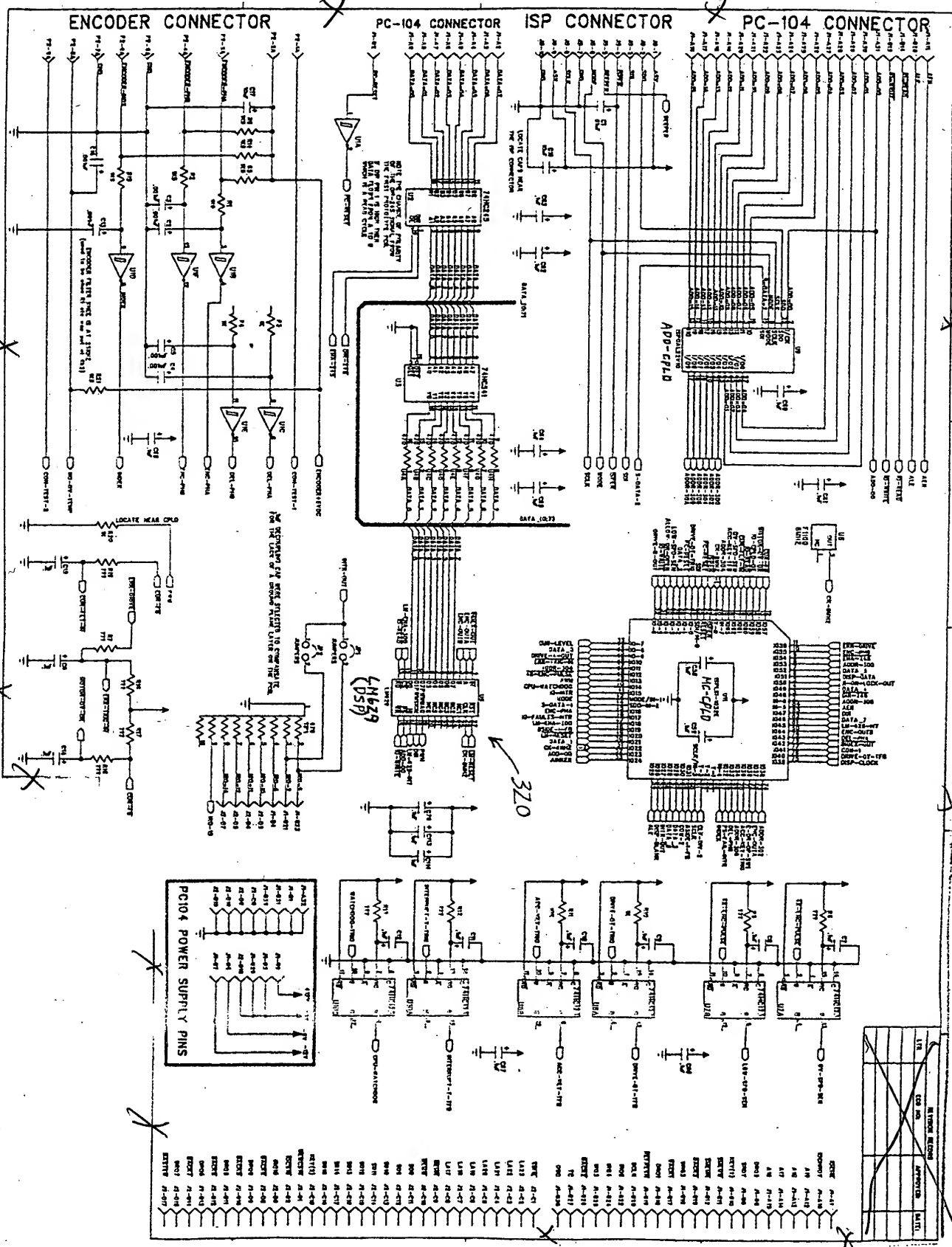
FIGURE 8A



MD-I/O CARD  
 LAYOUT 1

O I P E J C 4 2  
 JAN 3 0 2003  
 PATENT & TRADE MARK OFFICE

FIGURE 10B



MD-IP CARD  
 LAYOUT 2



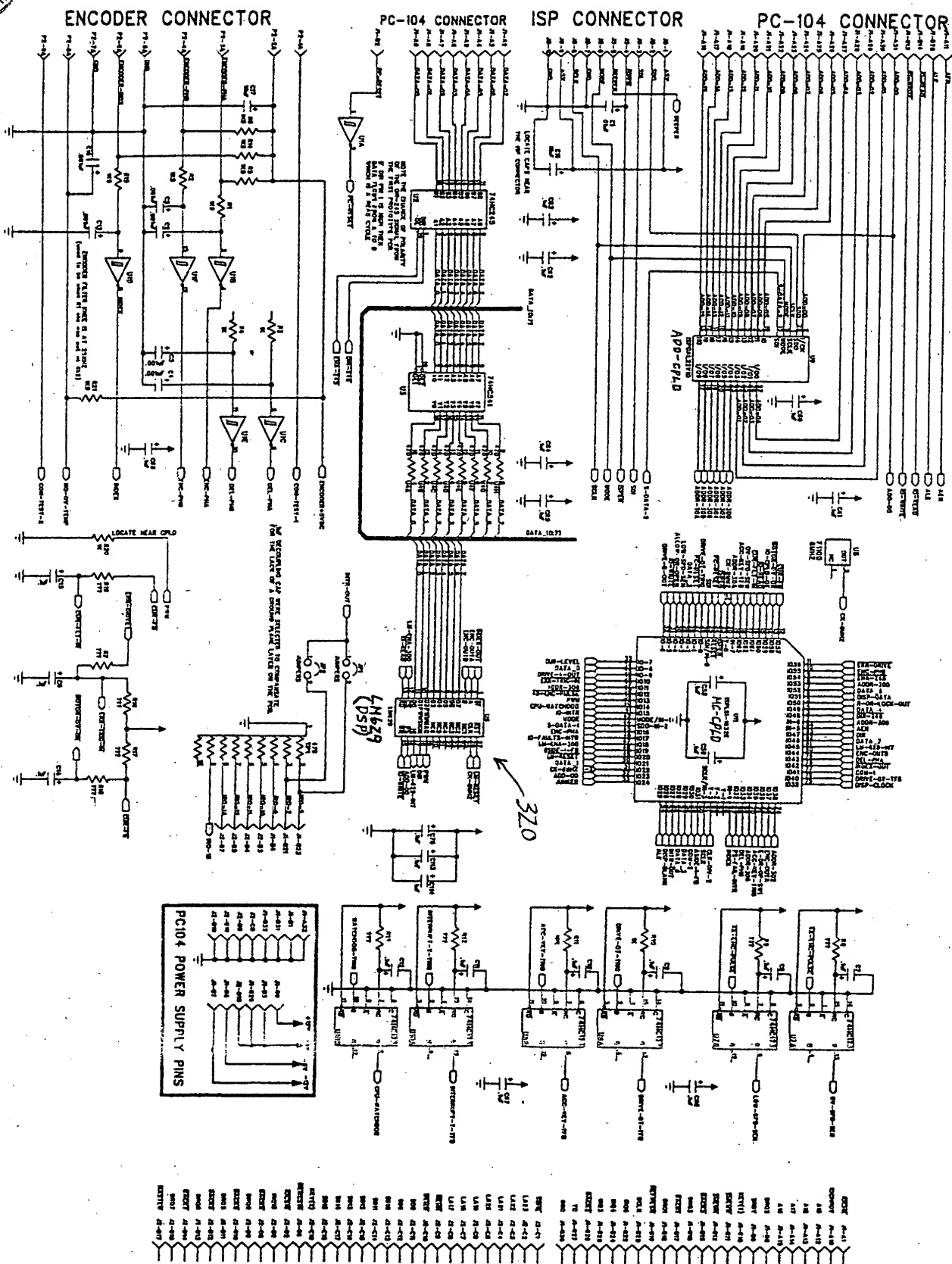
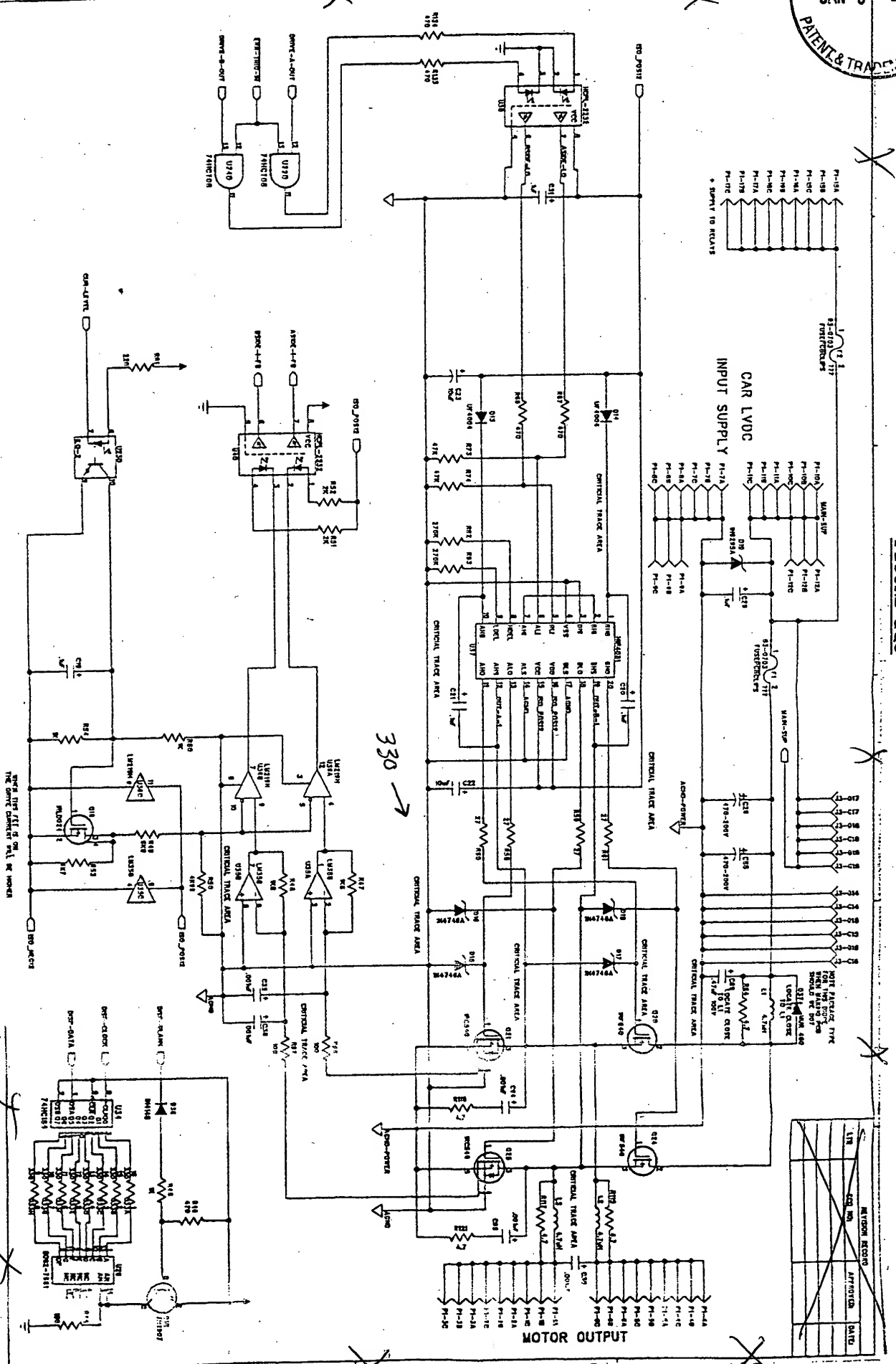


FIGURE 8 B

MD-IPb Card  
Layout Z

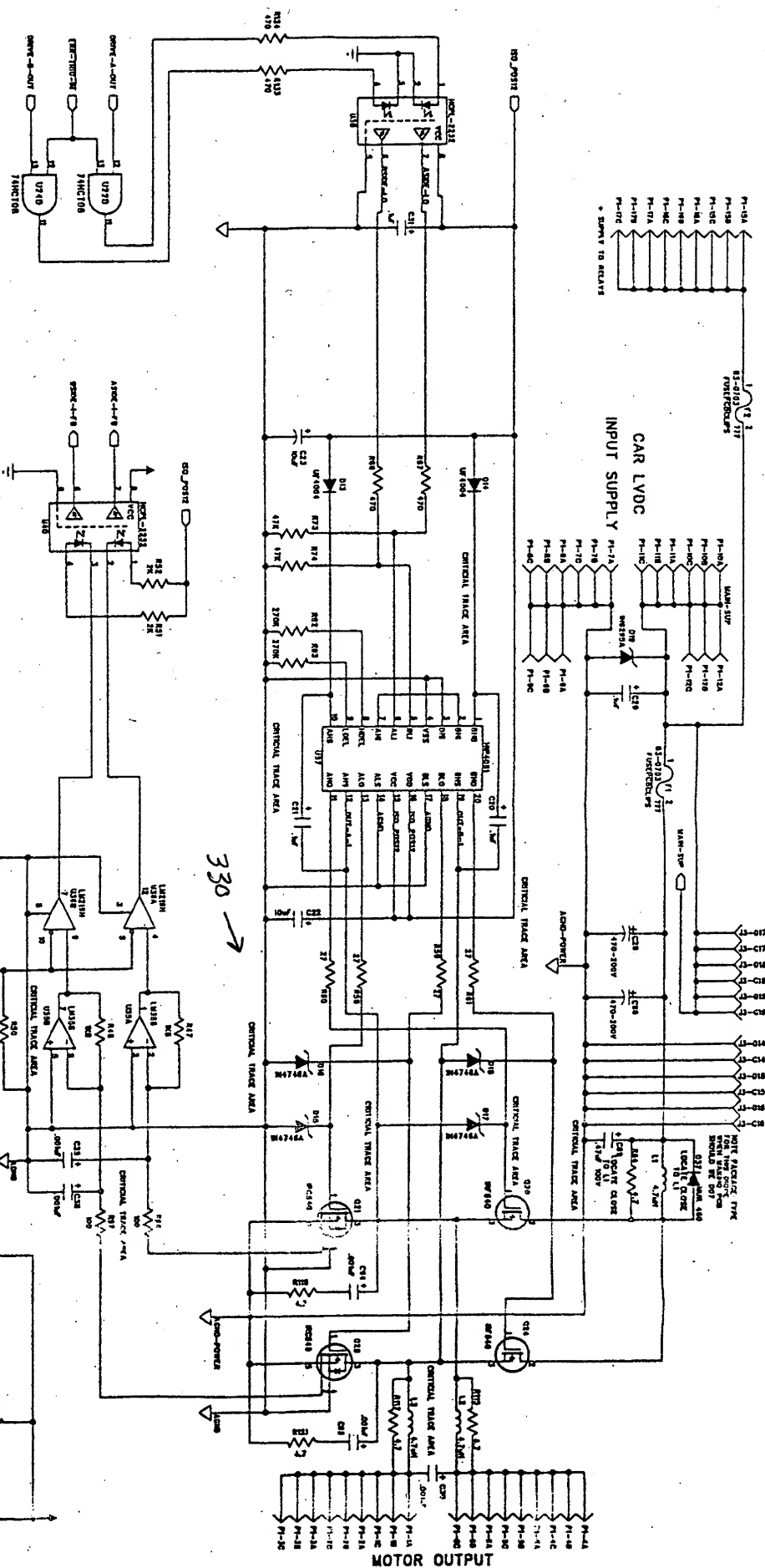
FIGURE 20C



WIRING CONNECTIONS

- P1-1A → P1-1B → P1-1C
- P1-1A → P1-1B → P1-1C
- P1-1A → P1-1B → P1-1C
- P1-1A → P1-1B → P1-1C

MD-1/0 CAPD  
Layout 3



**UNUSUS COMMERCION**

→ P-134  
→ P-138  
→ P-139

→ Pt-14A      → Pt-14B

→ P1-104  
→ P1-103  
→ P1-102

$$\begin{array}{ccc} \rightarrow P_1 - MA & \rightarrow P_1 - 100 & \rightarrow P_1 - 10 \end{array}$$

**MOTOR OUTPUT**

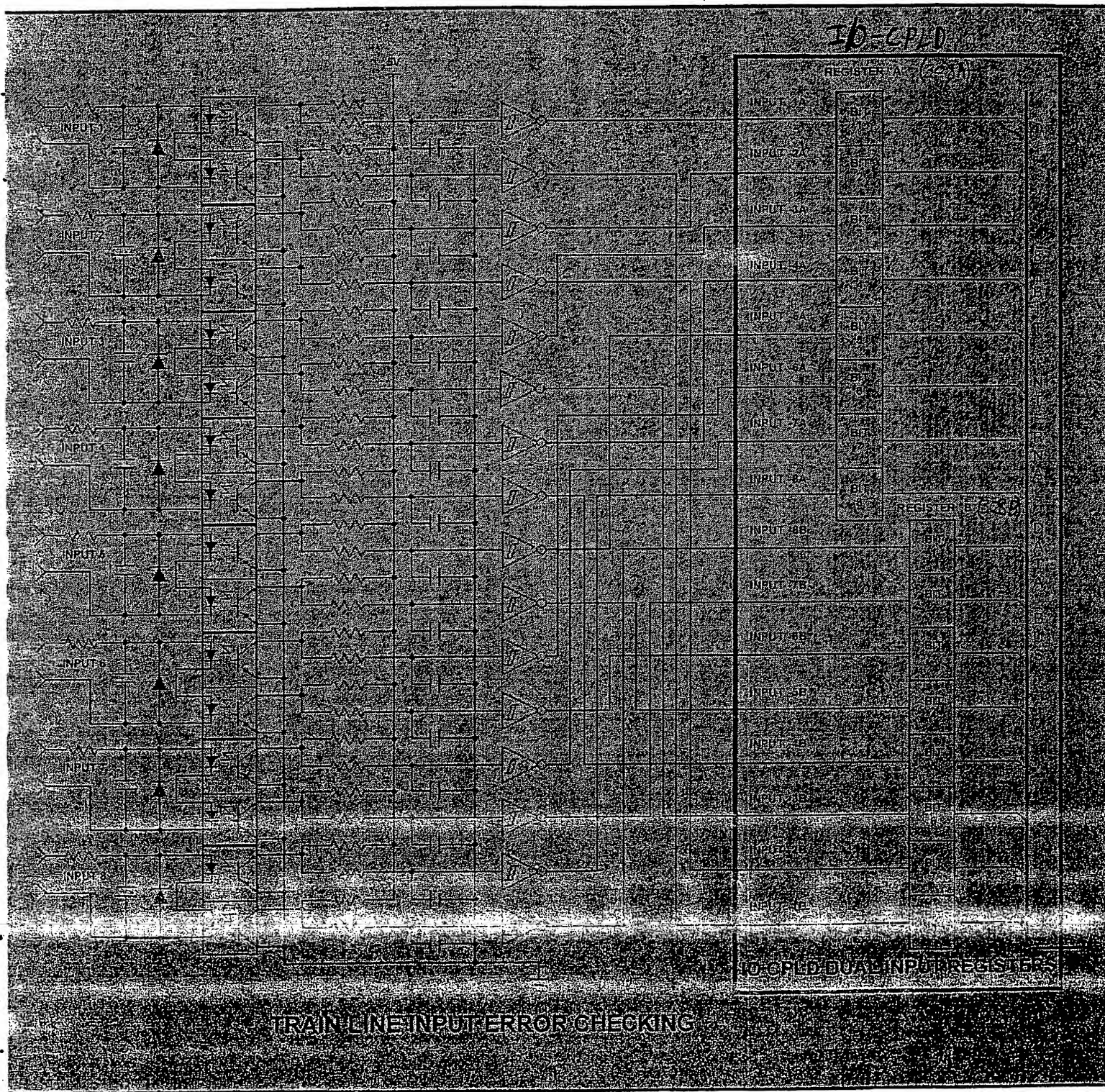
MD-I/O CARD  
Layout 3





FIGURE ~~A~~

310

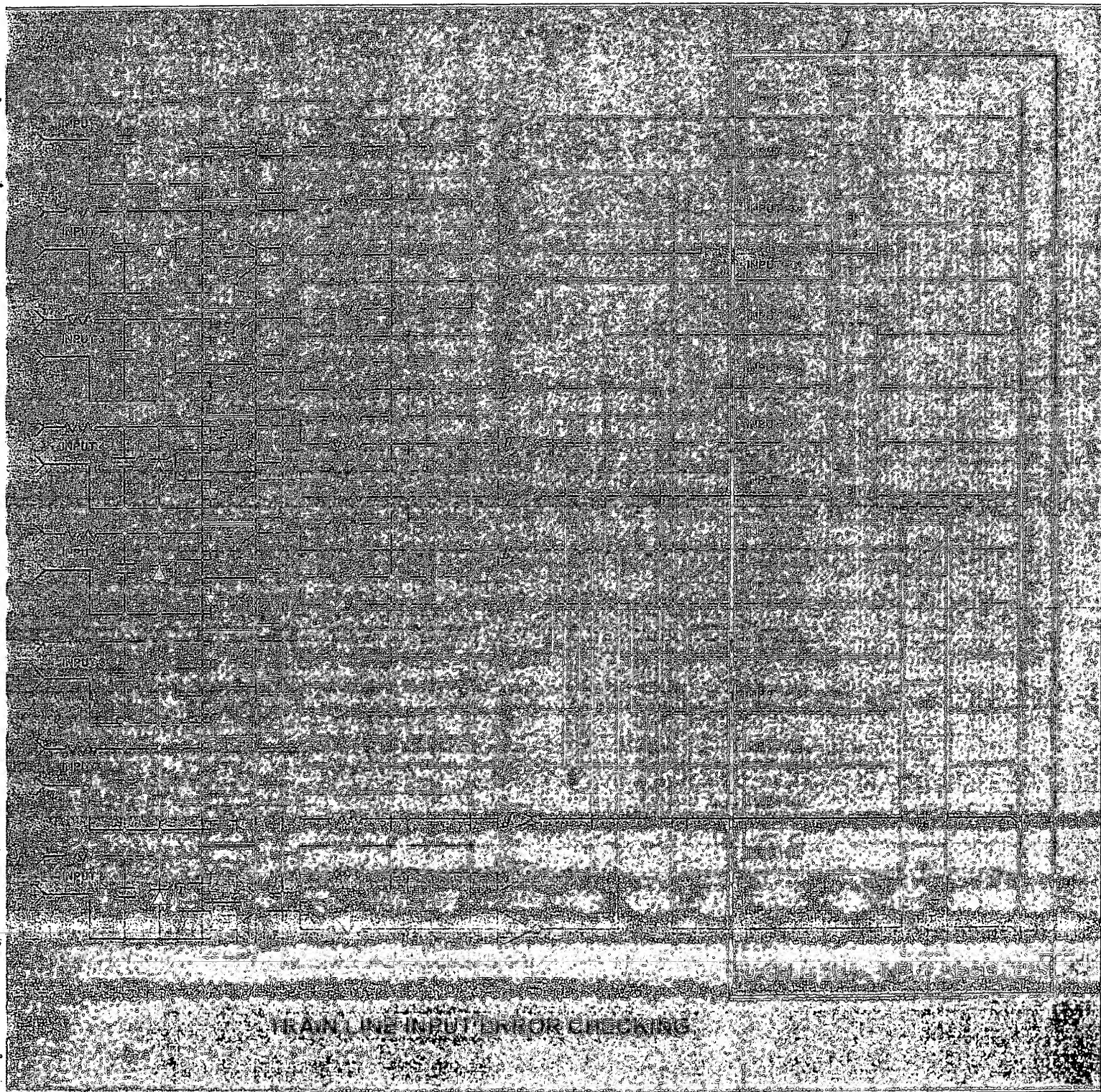




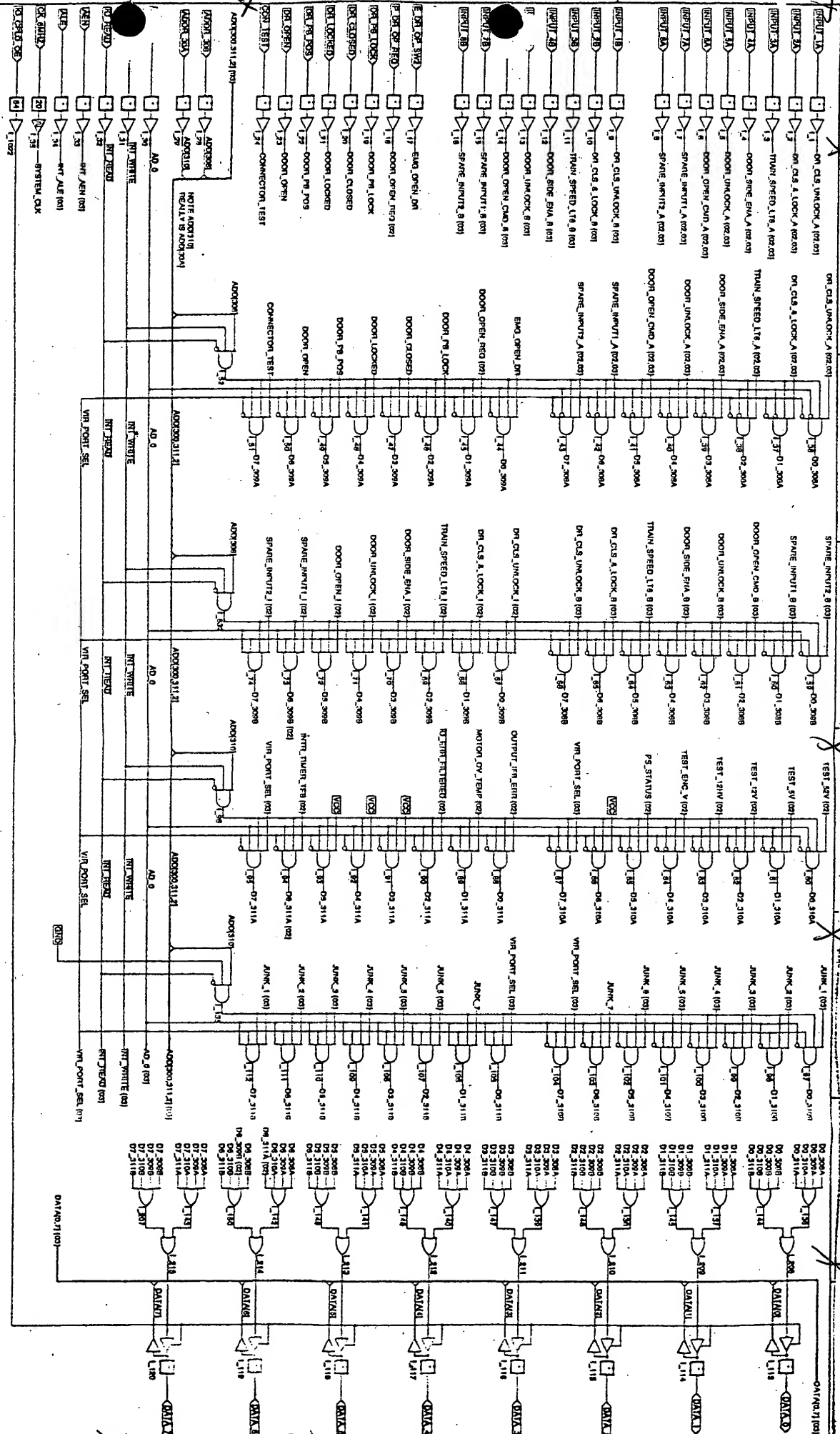
COPIED  
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FIGURE 9

310

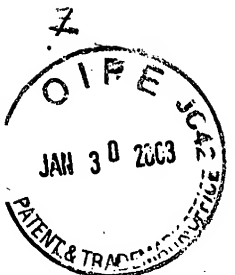


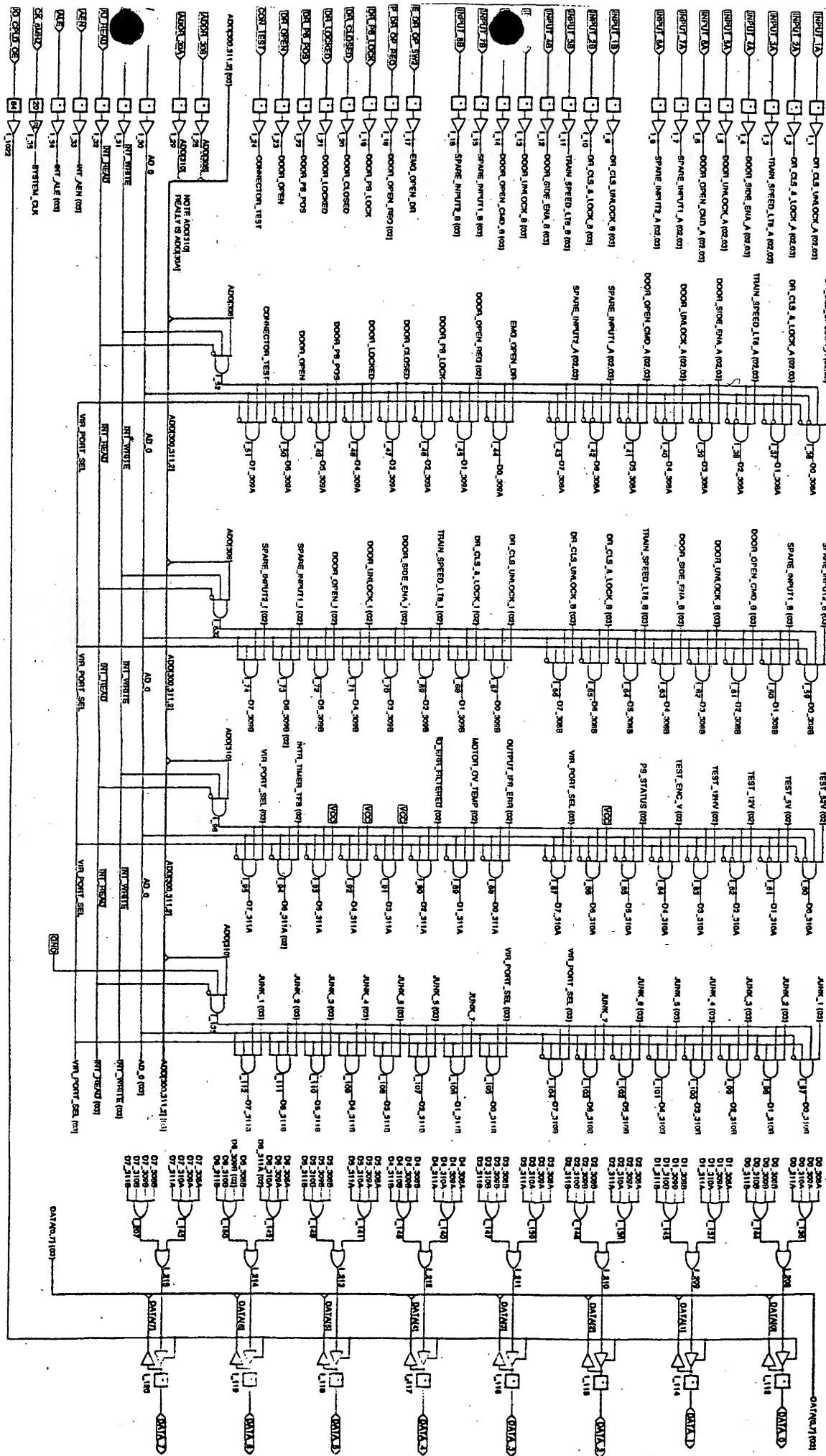
14.  $\frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$



MD-IT/CARD

I/O - CPLD DATA/ADDRESS  
CONTROL LOGIC





1000

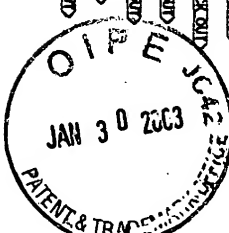
(I/O-CPLD DATA/ADDRESS CONTROL LOGIC)

DATA 0.71 0.01



MD-I/O CARD  
(I/O-CPLD DATA WRITE PORTS)

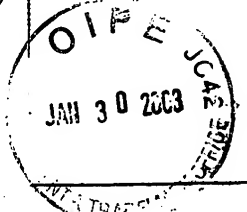
—OAT No. 7 (oil)



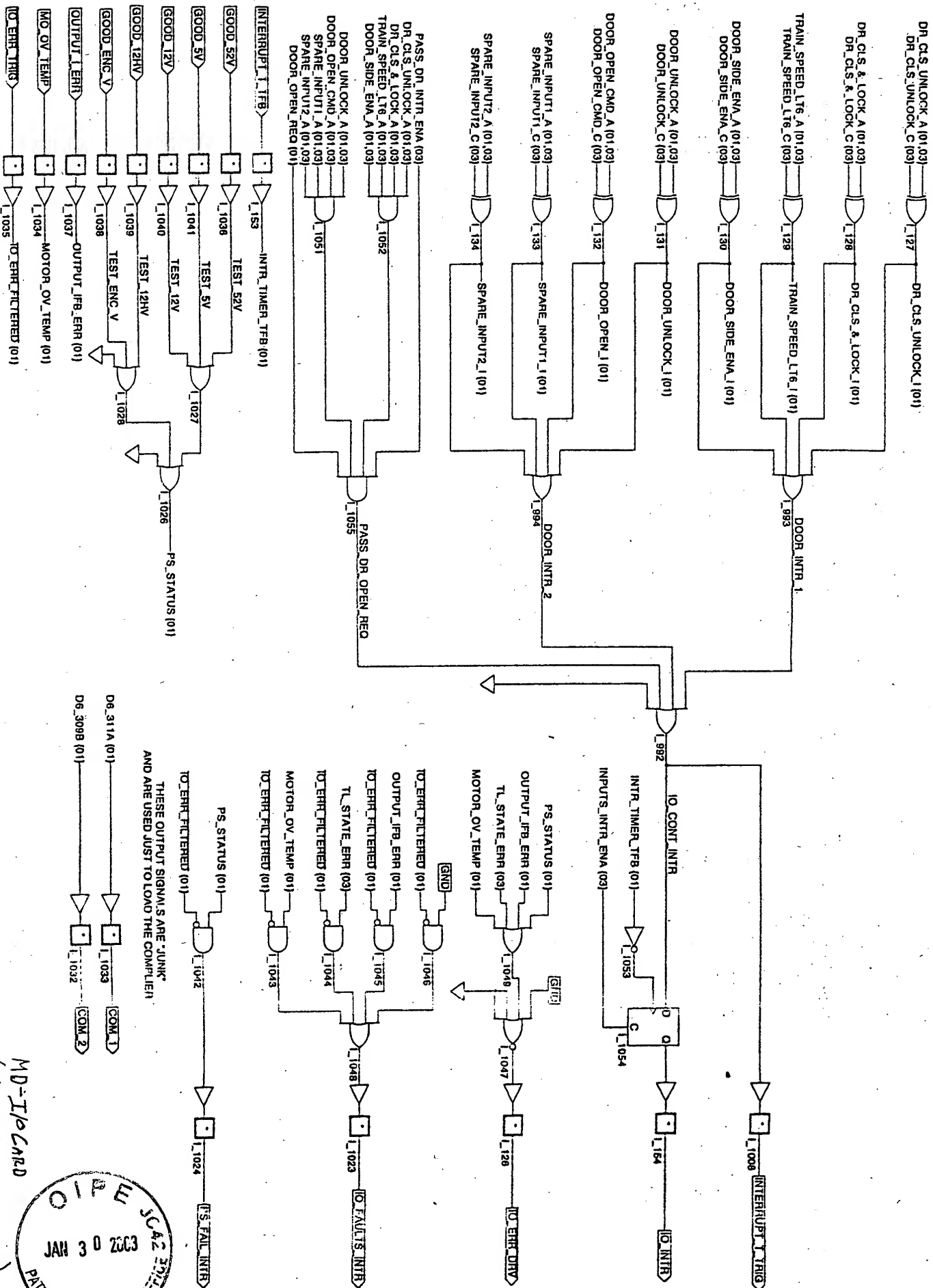
MD-I/O CARD  
(I/O-CPLD DATA WRITE PORTS)



**FIGURE 78C**



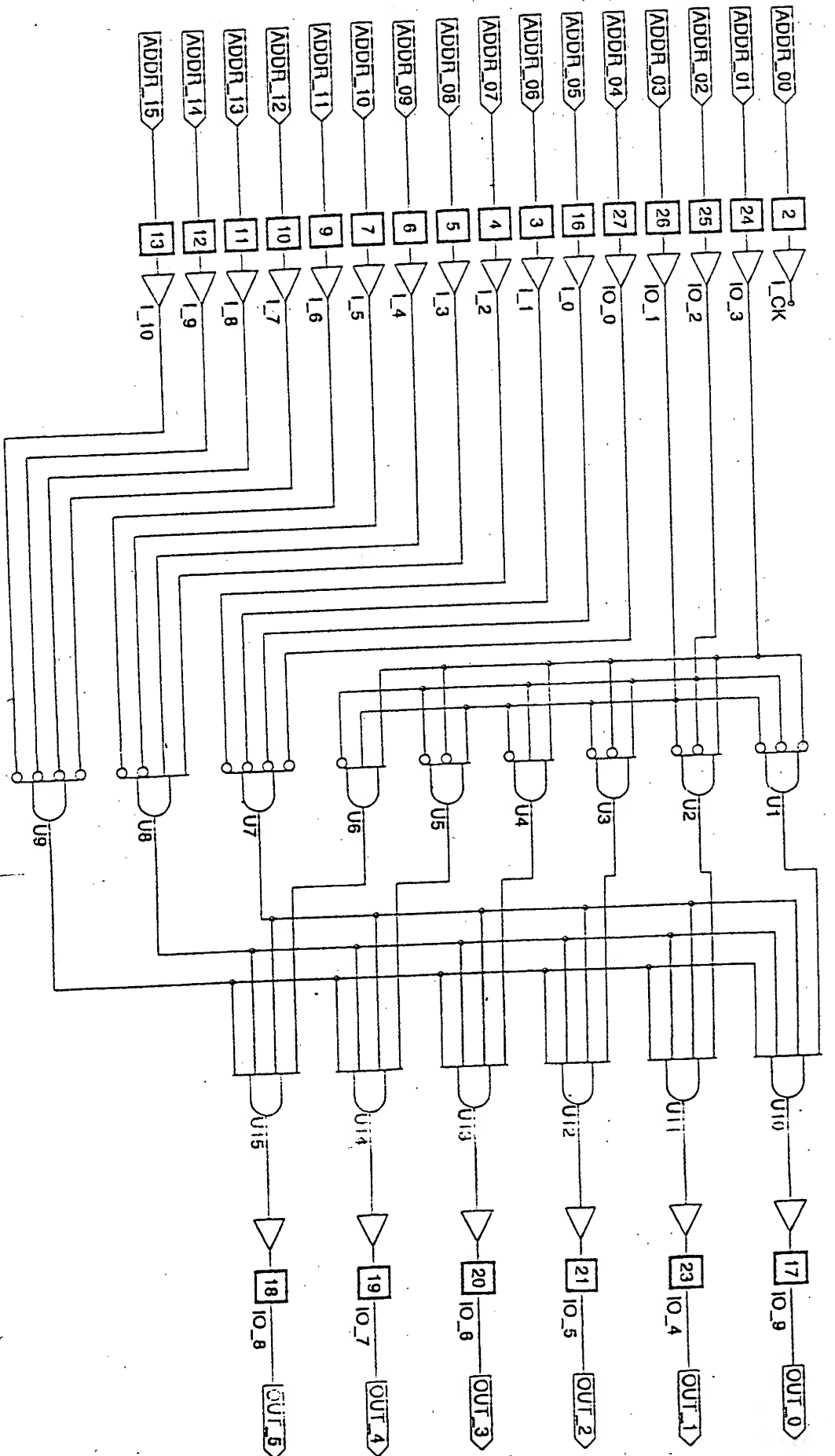
**FIGURE 10C**  
**INTERRUPT AND FILTER CONTROL CIRCUITS**



MD-1/0 CARD  
 I/O-CPLD INTERRUPT AND  
 FILTER CONTROL CIRCUITS

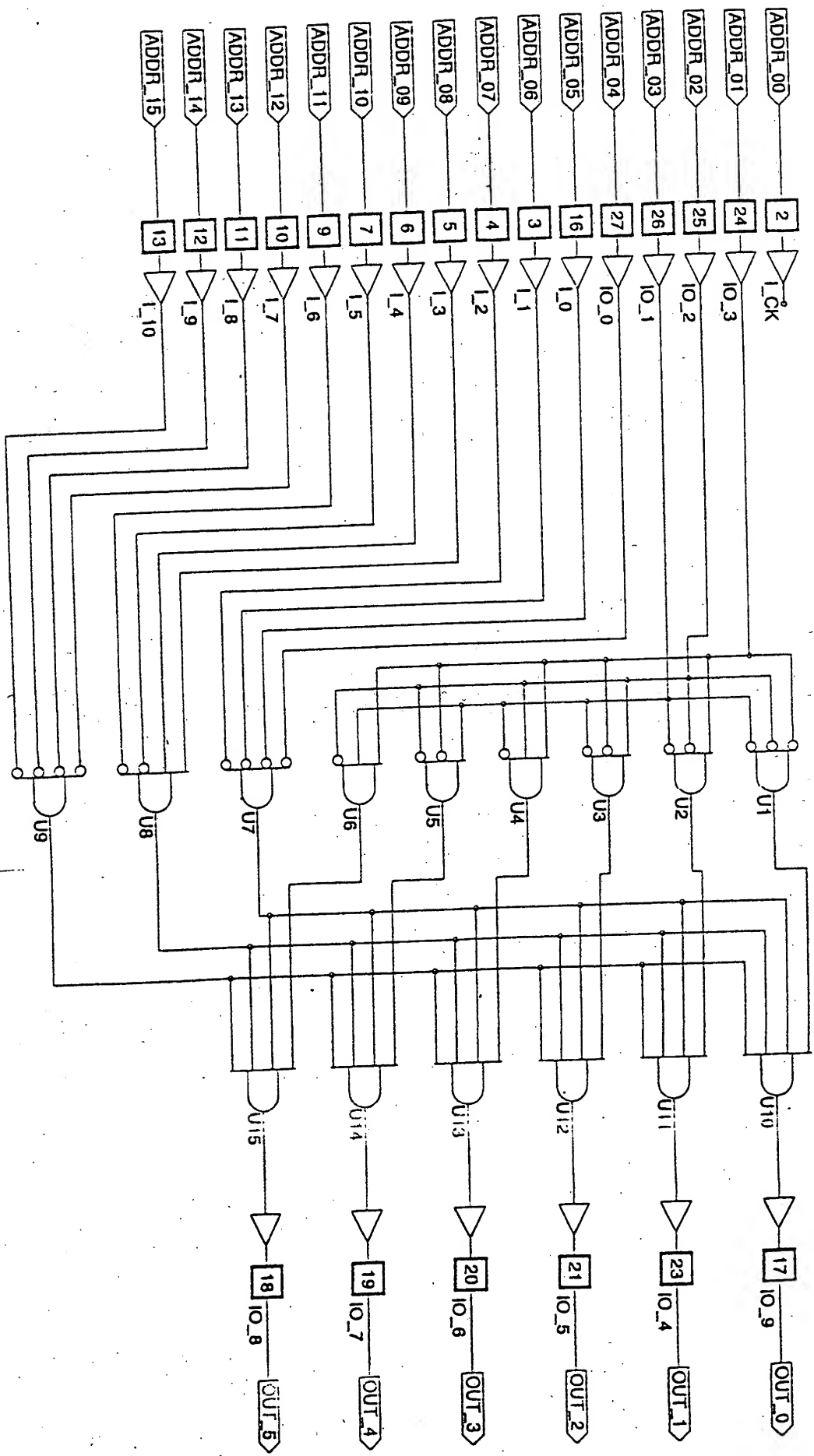


FIGURE 13



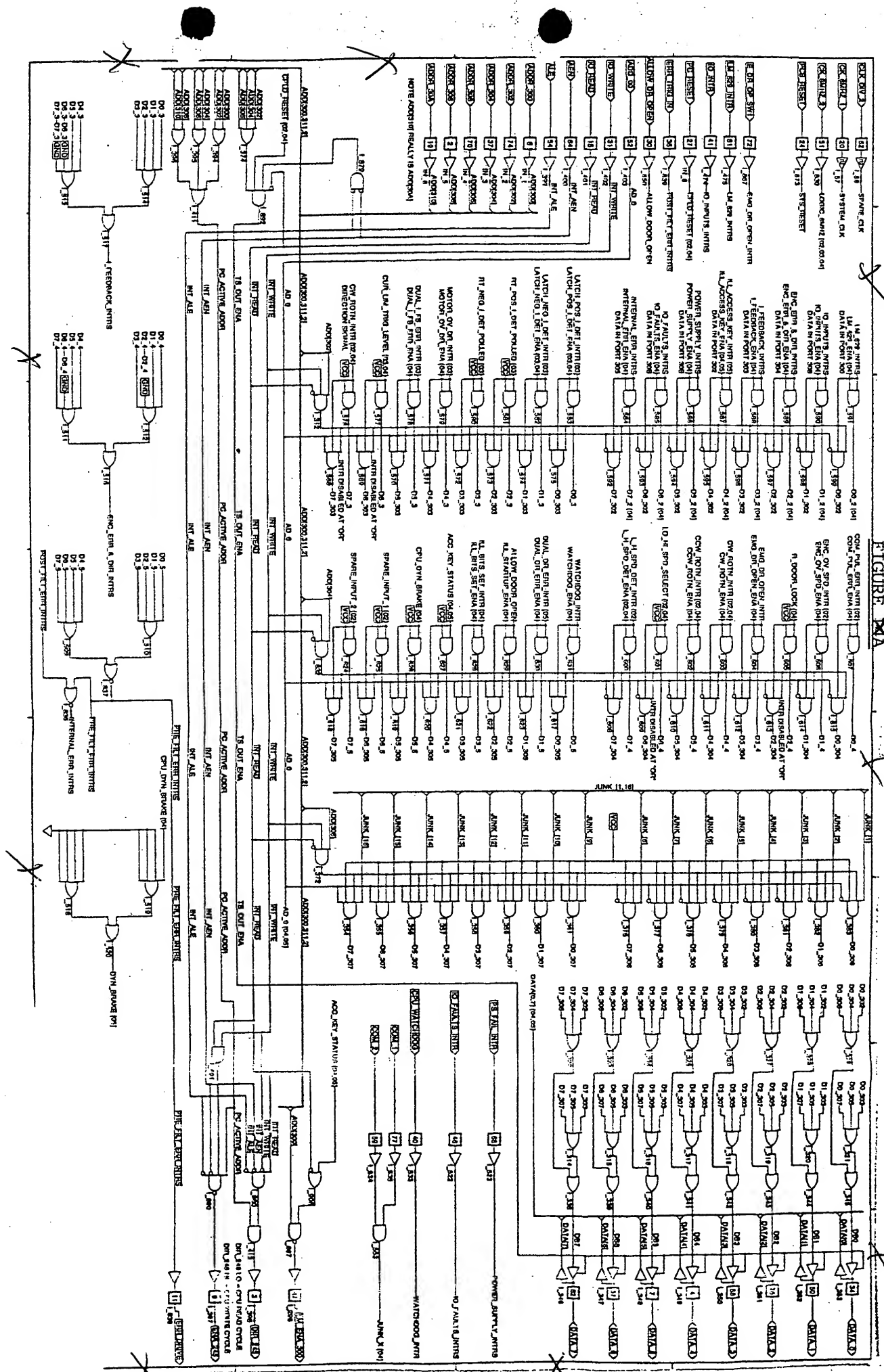
MD-I/O CARD  
(ADD-CPLD LOGIC)

FIGURE 11



MD-I/O CARD  
(ADD-CPLD LOGIC)

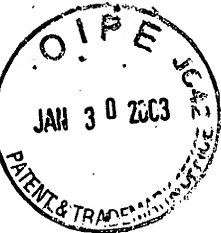
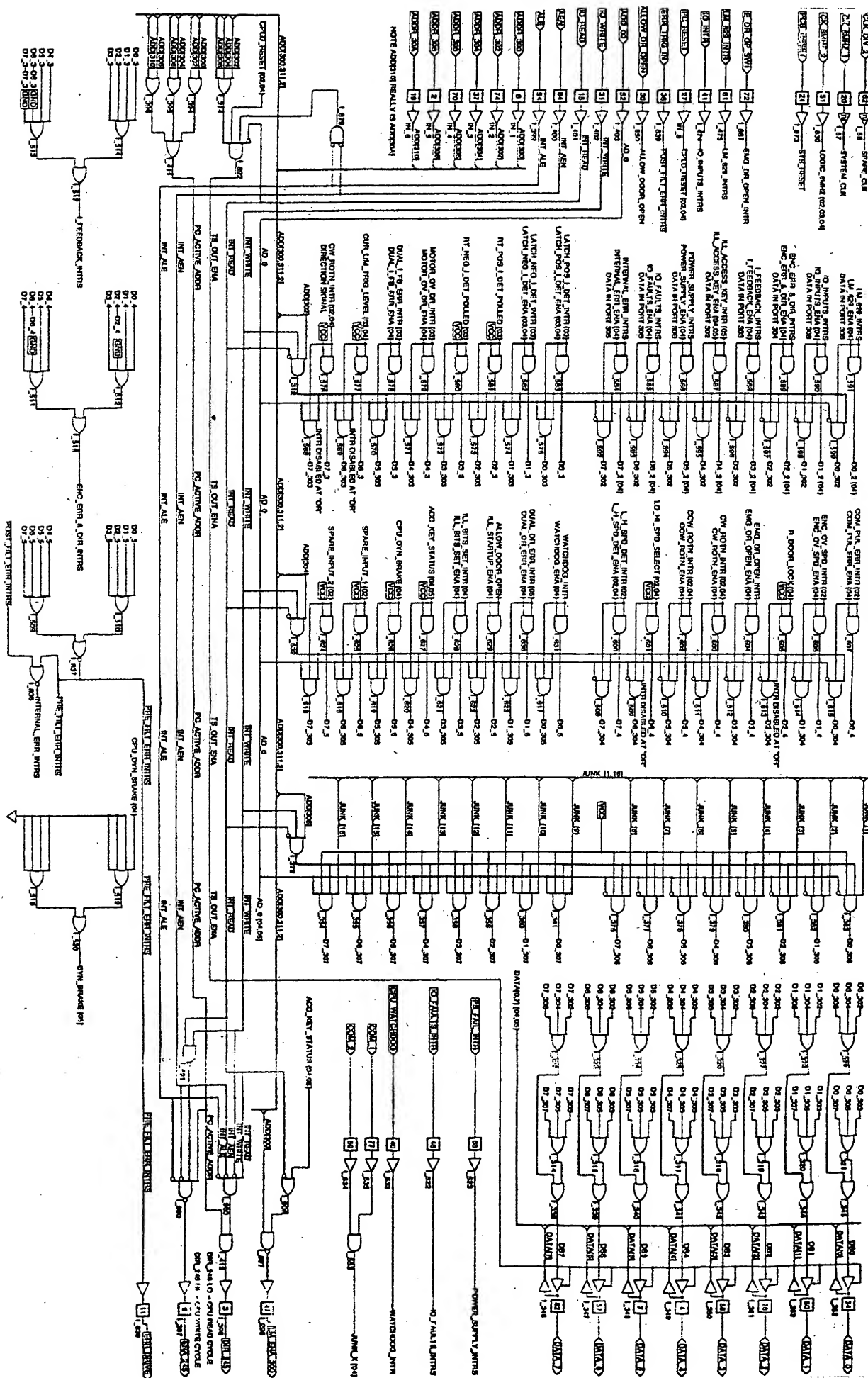




21A

MD-1/0 CAPD  
(MC-CPLD DATA/ADDRESS)  
CONTROL LOGIC

FIGURE 12A

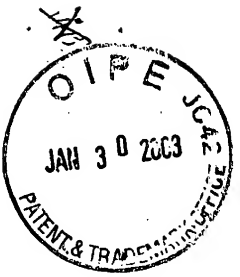
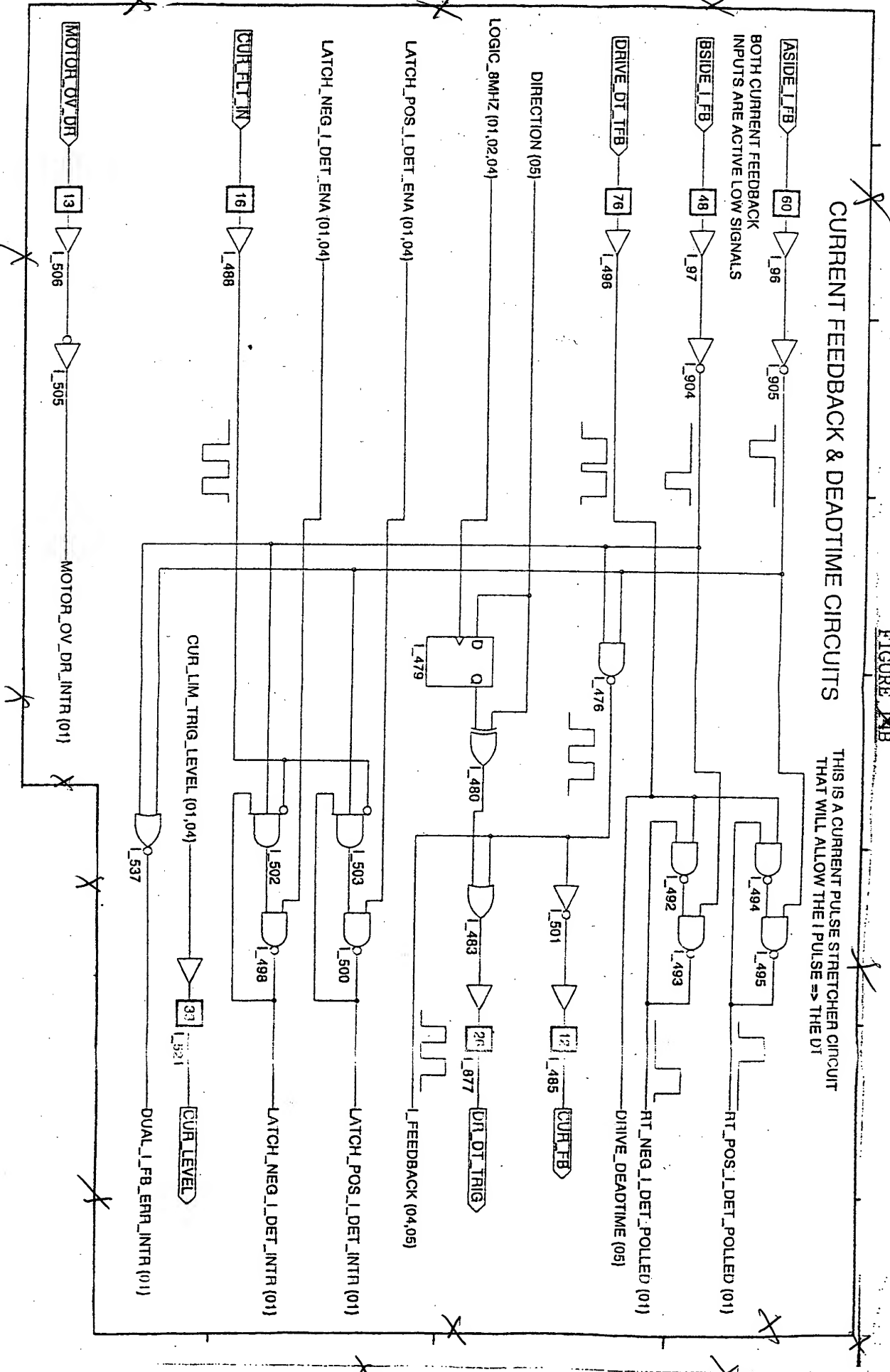


MD-110 CAPD  
(MC-CPLD DATA/ADDRESS)  
CONTROL LOGIC

FIGURE 14B

# CURRENT FEEDBACK & DEADTIME CIRCUITS

THIS IS A CURRENT PULSE STRETCHER CIRCUIT THAT WILL ALLOW THE I PULSE => THE DI

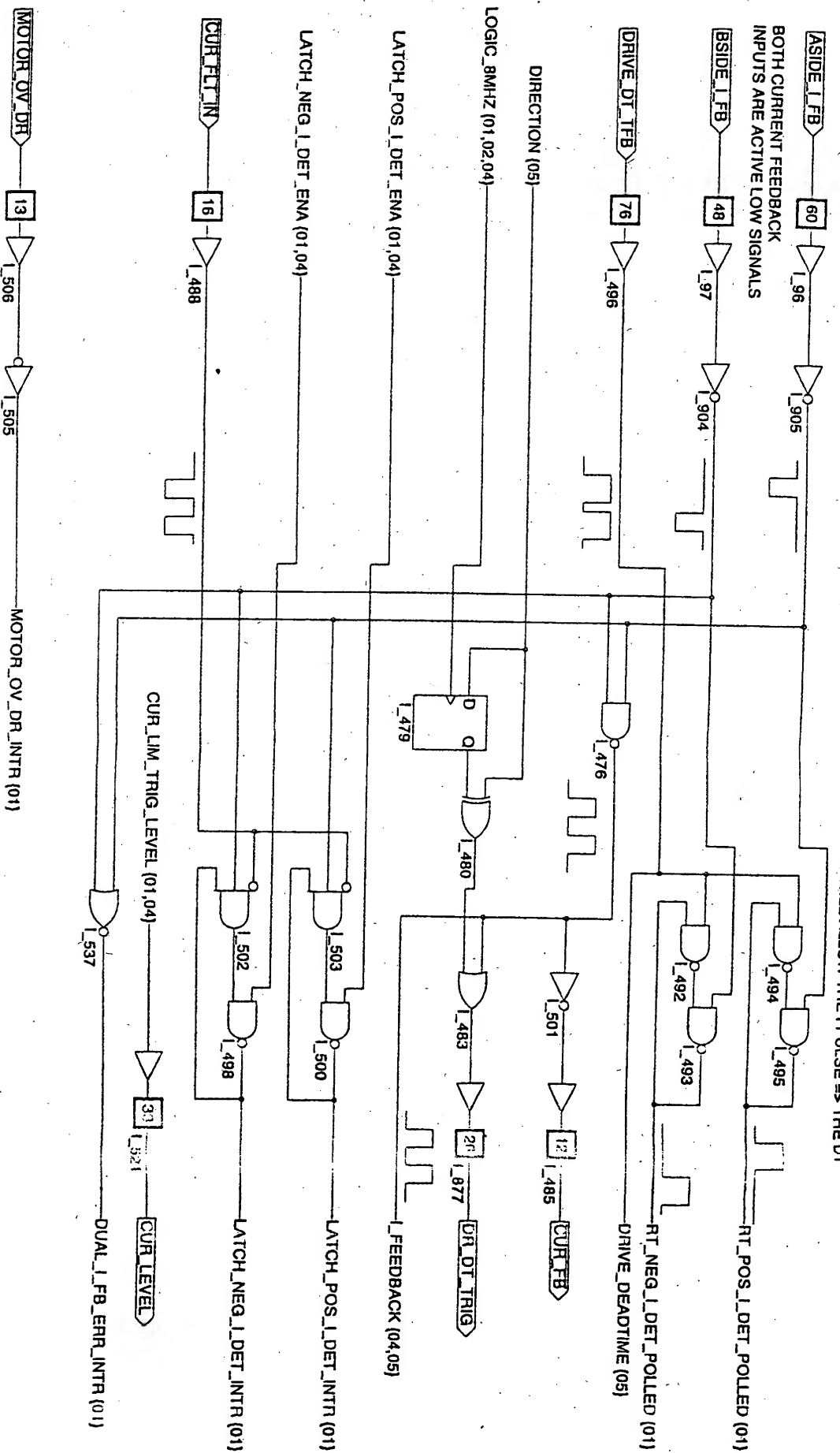


MD-I/O CARD  
(MC-CPLD Current Feedback  
AND DEADTIME CIRCUITS)

FIGURE 12B

# CURRENT FEEDBACK & DEADTIME CIRCUITS

THIS IS A CURRENT PULSE STRETCHER CIRCUIT THAT WILL ALLOW THE I PULSE => THE DI



MD-I/O CARD

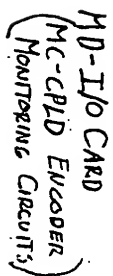
(MC-CPLD CURRENT FEEDBACK AND DEADTIME CIRCUITS)



## ENCODER MONITORING CIRCUITS



(MC-CPLD ENCODER  
MONITORING CIRCUITS)





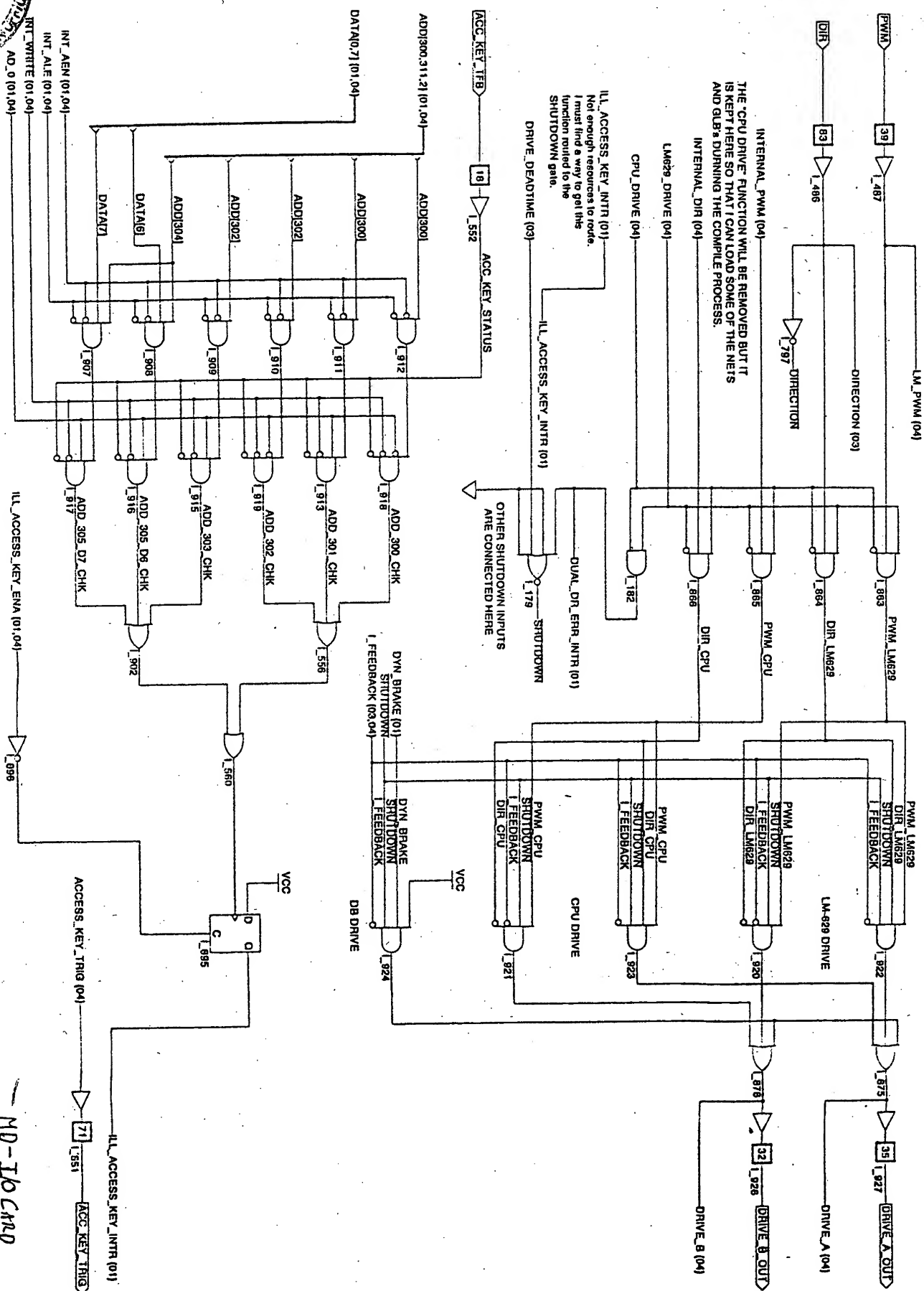
**FIGURE 1A-D**



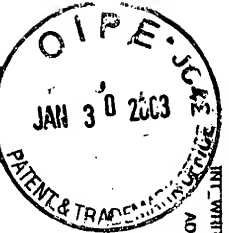
(MC-CPLD H-Bridge Control  
AND Access Key Control)

FIGURE 12D

"H" BRIDGE & ACCESS KEY CONTROL CIRCUITS

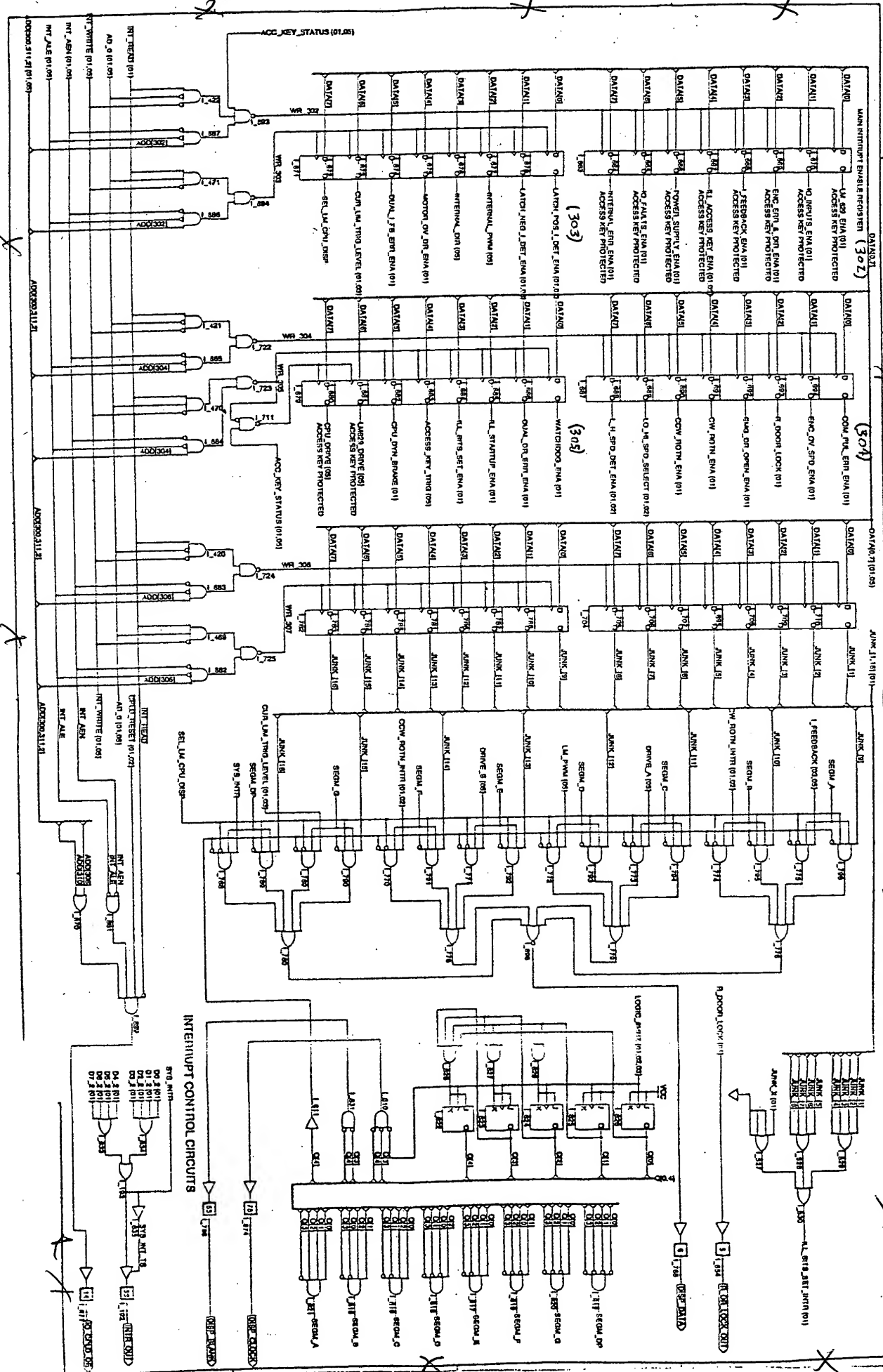


MD-I/O CARD  
(Mc-CPLD H-Bridge Control)  
AND Access Key Control



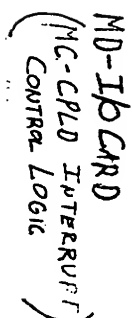
O I P E J C A Z  
 JAN 30 2003  
 PATENT & TRADE MARK

FIGURE ME



MD-10 CARD  
 (MC-CPLD INTERRUPT)  
 CONTRA LOGIC

A circular ink stamp from the U.S. Patent and Trademark Office. The date "JAN 30 2003" is stamped in the center. The words "U.S. PATENT &amp; TRADEMARK OFFICE" are curved along the top and right edges of the circle.



(MC-CPLD INTERRUPT  
CONTRA LOGIC)

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